EPEEC: Comprehensive SPICE-Compatible Reluctance Extraction for High-Speed Interconnects above Lossy Multilayer Substrate

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***Abstract*— With continuous advances in radio frequency (RF) mixed-signal very large scale integration (VLSI) technology, the creation of eddy currents in lossy multilayer substrates has made the already complicated interconnect analysis and modeling issue more challenging. To account for substrate losses, traditional electromagnetic methods are often computationally prohibitive for today's VLSI geometries. In this paper, an accurate and efficient interconnect modeling approach – EPEEC (Eddy-current-aware Partial Equivalent Element Circuit) – is proposed. Based on complex image theory, it extends the traditional partial equivalent element circuit (PEEC) model to simultaneously take multilayer substrate eddy current losses and frequency dependent effects into consideration. To accommodate even larger scale on-chip interconnect networks, EPEEC develops a new SPICE-compatible reluctance extraction algorithm by applying sparsification in the inverse inductance domain with an extended window algorithm. Comparing with several industry standard inductance and full-wave solvers, such as FastHenry and Sonnet®, EPEEC demonstrates within 1.5% accuracy while providing over $100X$ speedup.**

***Index Terms*— Interconnect, substrate, eddy current, interconnect modeling, inductance extraction, parasitic extraction, reluctance, complex image theory.**

I. Introduction

THE industry trend of integrating higher levels of circuit functionality on one chip and the widespread growth of wireless communication have triggered the proliferation of mixed analog-digital systems. However, the development of efficient interconnect models for such a system is made more difficult because of the lossy nature of the silicon substrate. In particular, the creation of substrate eddy currents can lead to considerable interconnect inductive and ohmic losses. As the behavior of on-chip interconnects becomes a dominant factor in overall circuit performance at high frequencies, an interconnect system analysis without considering the lossy substrate effects will result in an over-designed network and seriously waste chip resources [1].

With the increasing clock frequency and integration density, intentional and unintentional inductive effects gradually rise in VLSI design. Inductance computation is a difficult task since inductance depends on the current return path, which is unknown prior to the extraction and simulation of a circuit model [2]–[4].

Fortunately, the PEEC method has been widely adopted to deal with this issue [5]. However, since PEEC assumes that each conductor segment has a current return path at infinity, inductive couplings are now among all conductor segments, so that extremely dense partial inductance matrices are usually generated. For this reason, the reluctance-based method [6], [7] has been proposed by Hao Ji et al to alleviate this problem. Since reluctance has higher degree of locality similar to capacitance, only a small number of neighbors need to be considered. Consequently, the reluctance matrix for circuit simulation is very sparse compared to the partial inductance matrix.

Moreover, the traditional PEEC approach does not take substrate effects into consideration, and hence cannot capture inductive and ohmic losses due to the formation of eddy currents in the conductive substrate. Although several previous works have been proposed to resolve this issue by constructing three dimensional linear substrate models, such as [8]–[14], most of these approaches are based on the numerical finite difference method. With the roaring clock frequency and the reduced substrate resistivity, a large volume of silicon bulk needs to be spatially discretized into very tiny cells to capture the substrate effects accurately. Therefore, the obtained equivalent circuit models are extremely prohibitive in sizes since inductive couplings are now among all conductor segments and substrate cells.

In this paper, we propose EPEEC, an accurate, compact, and efficient interconnect modeling methodology to extend the PEEC model to consider multilayer substrates based on complex image theory [15], which has recently been used in RFIC regime to consider microstrips and spiral conductors over a single layer substrate [16]–[18]. To deal with multilayer substrates, we present the detailed methodology to derive the effective complex distance (ECD) between physical conductors and their corresponding complex images by preserving the first moment of the analytic vector potential formulation. The EPEEC model is obtained by modifying PEEC with mutual inductances between physical and image conductors separated by the effective complex distance. Since EPEEC reflects the substrate effects in resistance and inductance values directly based on the configuration of substrate instead of applying discretization, it leads to very compact models for interconnects.

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For modeling even larger scale interconnect systems, EPEEC is enhanced to extract reluctance instead of inductance by applying an extended window-based reluctance extraction algorithm. Furthermore, we propose a reluctance realization algorithm by directly converting reluctances to circuit elements compatible with general circuit simulators, such as SPICE.

After validating the EPEEC model by comparison with the rigorous full-wave simulator, Sonnet®, we use EPEEC to comprehensively study the impacts of frequency and substrate configuration, such as thickness and conductivity, on interconnect models.

We have clearly supported the motivation for the new interconnect modeling methodology. The discussion proceeds (Section II) with describing the application of complex image theory to on-chip interconnects above a lossy multilayer substrate. Section III presents the EPEEC model based on the derived effective complex distance. Meaningful experimental results (Section IV) and a summary of our work (Section V) conclude this paper.

II. Electromagnetic Formulation of Substrate Eddy Current and Complex Image Theory

In this section, we explain the generation and the nature of eddy currents in a multilayer substrate. The effective complex distance can be obtained by preserving the first moment of the analytic vector potential formulation. Then we discuss the application of complex image theory to on-chip interconnects above a lossy multilayer substrate.

A. Generation of Substrate Eddy Currents

Eddy currents in the substrate are caused by time-varying magnetic fields. If a time-varying magnetic flux density $\mathbf{B}_f$ is induced by currents in interconnects, an electric field $\mathbf{E}$ is produced in the substrate as

$$\bigtriangledown \times \mathbf{E} \quad = \quad -\frac{\partial \mathbf{B}_f}{\partial t}. \tag{1}$$

The electric field $\mathbf{E}$ can be expressed in terms of the vector magnetic potential $\mathbf{A}$ and the scalar potential ϕ by

$$\mathbf{E} \quad = \quad -\frac{\partial \mathbf{A}}{\partial t} - \bigtriangledown \phi. \tag{2}$$

This electric field $\mathbf{E}$ in turn establishes currents flowing according to Ohm's law

$$\mathbf{J} \quad = \quad \sigma \mathbf{E}. \tag{3}$$

Substituting Eq. 3 into Eq. 2 leads to

$$\mathbf{J} \quad = \quad -\sigma(\frac{\partial \mathbf{A}}{\partial t} + \bigtriangledown \phi). \tag{4}$$

These induced currents will produce another magnetic field according to Ampere's Law

$$\bigtriangledown \times \mathbf{B} \quad = \quad \mu(\mathbf{J} + \frac{\partial \mathbf{D}}{\partial t}). \tag{5}$$

By using Eq. 3 and applying the constitutive equation $\mathbf{D} = \epsilon \mathbf{E}$, the time-harmonic format of Ampere's Law can be expressed as: $\bigtriangledown \times \mathbf{B} = \mu(\sigma \mathbf{E} + j\omega\epsilon \mathbf{E})$. Since at current frequencies of interest (< 20GHz), $\sigma >> \omega\epsilon$, the second term representing the displacement currents is at least three orders of magnitude smaller than the first term and can be safely ignored. Therefore, Ampere's Law in Eq. 5 can be simplified as

$$\bigtriangledown \times \mathbf{B} \quad = \quad \mu \mathbf{J}. \tag{6}$$

Since the magnetic flux density $\mathbf{B}$ is solenoidal, we have $\bigtriangledown \cdot \mathbf{B} = 0$. Substituting Eq. 4 into Eq. 6 and applying vector identities $\bigtriangledown \times (\bigtriangledown \times \mathbf{F}) = \bigtriangledown(\bigtriangledown \cdot \mathbf{F}) - \bigtriangledown^{\mathbf{2}}\mathbf{F}$ and $\bigtriangledown \times \bigtriangledown \phi = 0$, it can be obtained that

$$\bigtriangledown^2 \mathbf{B} - \mu\sigma \frac{\partial \mathbf{B}}{\partial t} \quad = \quad 0. \tag{7}$$

Eq. 7 is referred to as the diffusion equation in terms of the magnetic flux density $\mathbf{B}$.

From Eq. 7, one can see that although the current arising from the electrical potential ϕ in Eq. 4 could be as large as the current arising from the magnetic vector potential $\mathbf{A}$, its contribution to the magnetic flux density can be ignored by noticing that $\bigtriangledown \times \bigtriangledown \phi = 0$. Furthermore, since the magnetic flux density $\mathbf{B}$ determines the magnetic flux Φ, and hence directly affects the line parameter $L = \Phi / I$, we do not need to consider the current arising from the electrical potential ϕ [19], [20], and in this scenario, Eq. 4 can be approximated as

$$\mathbf{J} \quad = \quad -\sigma \frac{\partial \mathbf{A}}{\partial t}. \tag{8}$$

Substituting $\mathbf{B} = \bigtriangledown \times \mathbf{A}$ into Eq. 6 and adopting Coulomb gauge $\bigtriangledown \cdot \mathbf{A} = 0$ leads to

$$\bigtriangledown^2 \mathbf{A} \quad = \quad -\mu \mathbf{J}. \tag{9}$$

By using Eq. 8 and Eq. 9, we get

$$\bigtriangledown^2 \mathbf{A} - \mu\sigma \frac{\partial \mathbf{A}}{\partial t} \quad = \quad 0. \tag{10}$$

Eq. 10 is the diffusion equation of the vector potential in a medium subject to a time-varying magnetic field.

B. Analytic Vector Potential within A Multilayer Substrate

Outside the diffusion/active areas and contact areas, the substrate can be treated as consisting of uniformly-doped semiconductor-material layers of varying doping densities [10].

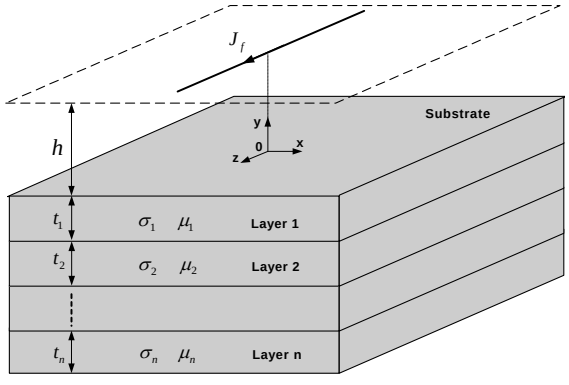

Fig. 1. A current filament parallel to a multilayer substrate which contains different layers of different thickness, conductivity, and permeability.

Assume that a long current filament is located distance h above a multilayer substrate. Current density within the filament is denoted by $\mathbf{J}_f$. The substrate consists of n layers. The layer k in the substrate has thickness t_k, conductivity σ_k, permeability μ_k, and is assumed infinite in the traverse direction. Regions above and below substrate are free spaces. The configuration is shown in Fig. 1.

For frequencies up to a few giga-Hertz, we can make magneto-quasi-static assumption. Under this assumption, induced eddy currents within the substrate will be parallel to the filament. For a z-direction filament current, only the z-component of $\mathbf{A}$ is nonzero, so that the problem becomes two dimensional. By using Eqs. 9 and 10, we can obtain magnetic vector potential diffusion equations in different regions

$$\begin{cases} \bigtriangledown^2\mathbf{A}_0(x,y) = -\mu_0\delta(0,y-h)\mathbf{J}_f & \text{Above Substrate,} \\ \bigtriangledown^2\mathbf{A}_k(x,y) = j\omega\mu_k\sigma_k\mathbf{A}_k(x,y) & \text{Within Substrate,} \\ \bigtriangledown^2\mathbf{A}_{n+1}(x,y) = 0 & \text{Below Substrate,} \end{cases} \quad (11)$$

where $k = 1, \cdots, n$. $\mathbf{A}_k$ denotes the vector potential within the substrate layer k.

Applying the method of separation variables and noticing the symmetry of the configuration with respect to the y axis [19], [21], it can be shown that the general solution of Eqs. 11 is given by

$$\mathbf{A}_k(x,y) = \int_0^\infty \left[M_k(\tau)e^{\gamma_k y} + N_k(\tau)e^{-\gamma_k y}\right] cos(\tau x)d\tau, \quad (12)$$

where

$$\begin{aligned} \gamma_k &= (\tau^2 + \zeta_k^2)^{1/2}, \\ \zeta_k &= \sqrt{j\omega\mu_k\sigma_k}. \end{aligned} \quad (13)$$

To solve vector potentials in the whole problem space, there are $2(n+2)$ unknown M_k's and N_k's in Eq. 12. In order to obtain those coefficients, we need to apply boundary conditions at different medium interfaces. Since the normal component of the flux density and the tangential component of the field intensity are continuous, we obtain that for the boundary between the substrate layer k and $k+1$

$$\begin{aligned} \mathbf{B}_{k,y} &= \mathbf{B}_{k+1,y}, \\ \frac{1}{\mu_k}\mathbf{B}_{k,x} &= \frac{1}{\mu_{k+1}}\mathbf{B}_{k+1,x}. \end{aligned} \quad (14)$$

Since $\mathbf{B} = \bigtriangledown \times \mathbf{A}$ and only the z-component of $\mathbf{A}$ is nonzero, by using Eq. 12, the x and y components of the magnetic flux density will be

$$\begin{aligned} \mathbf{B}_{k,x} &= \int_0^\infty \left[M_k e^{\gamma_k y} - N_k e^{-\gamma_k y}\right]\gamma_k cos(\tau x)d\tau, \\ \mathbf{B}_{k,y} &= \int_0^\infty \left[M_k e^{\gamma_k y} + N_k e^{-\gamma_k y}\right]\tau sin(\tau x)d\tau. \end{aligned} \quad (15)$$

By employing the boundary conditions in Eqs. 14, the coefficients of different substrate layers can be shown to have the following relationship [22]

$$\begin{bmatrix} M_{k+1} \\ N_{k+1} \end{bmatrix} = \frac{1}{2}\begin{bmatrix} (1+\lambda_k)e^{-\alpha_k} & (1-\lambda_k)e^{-\beta_k} \\ (1-\lambda_k)e^{+\beta_k} & (1+\lambda_k)e^{+\alpha_k} \end{bmatrix}\begin{bmatrix} M_k \\ N_k \end{bmatrix},$$

where

$$\begin{aligned} \lambda_k &= \frac{\mu_{k+1}}{\mu_k}\cdot\frac{\gamma_k}{\gamma_{k+1}}, \\ \alpha_k &= (\gamma_{k+1} - \gamma_k)\cdot y_k, \\ \beta_k &= (\gamma_{k+1} + \gamma_k)\cdot y_k, \end{aligned} \quad (16)$$

and $y_k = \sum_{i=1}^{k} t_k$ are the y coordinates of different interfaces.

Furthermore, by matching the magnetic flux generated by a current filament in free space, the coefficient M_0 can be obtained as

$$M_0(\tau) = \frac{\mu_0 I}{2\pi}\cdot\frac{e^{-h\tau}}{\tau}. \quad (17)$$

Also noticing that normally there is a ground plane underneath the substrate and for $y \to -\infty$, the field must vanish, we get

$$N_{n+1} = 0. \quad (18)$$

So we have $n+1$ interfaces and hence $2(n+1)$ boundary conditions to uniquely determine all the rest $2(n+1)$ unknown coefficients in Eq. 12 by using Eq. 16.

Since our purpose is to study the substrate effects on interconnects, we are interested in the vector potential in the region above substrate $(k = 0)$. The solution of the vector potential in this region can be shown to have the following general form

$$\mathbf{A}_0 = \frac{\mu_0 I}{2\pi}\int\left[\frac{e^{-\tau|y-h|}}{\tau} - \Gamma(\tau)\frac{e^{-\tau(y+h)}}{\tau}\right]cos(\tau x)d\tau \quad (19)$$

$\Gamma(\tau)$ is known after M_k's and N_k's are obtained using the above method.

C. Complex Image Theory and Its Application

It is observed that the integral in the analytic solution of $\mathbf{A}_0$ in Eq. 19 has two terms. The first term can be attributed to the current $\mathbf{J}_f$ following within the filament. The second term can be attributed to the induced substrate eddy currents [15]. So the vector potential can be written as

$$\mathbf{A}_0(x,y) = \mathbf{A}_0^f - \mathbf{A}_0^e, \quad (20)$$

where

$$\mathbf{A}_0^f = \frac{\mu_0 I}{2\pi}\int\frac{e^{-\tau|y-h|}}{\tau}cos(\tau x)d\tau, \quad (21)$$

$$\begin{aligned} \mathbf{A}_0^e &= \frac{\mu_0 I}{2\pi}\int\Gamma(\tau)\frac{e^{-\tau(y+h)}}{\tau}cos(\tau x)d\tau \\ &= \frac{\mu_0 I}{2\pi}\int\Gamma(\tau)e^{\tau d}\frac{e^{-\tau(y+h+d)}}{\tau}cos(\tau x)d\tau. \end{aligned} \quad (22)$$

The similarity between these two terms suggests that eddy currents induced in the substrate may be treated as an image filament current flowing at $y = -(h+d)$ in the opposite direction. This approximation holds when the coefficient $\Gamma(\tau)e^{\tau d}$ is approximated by constant one. The Taylor expansion of $\Gamma(\tau)e^{\tau d}$ at $\tau = 0$ is given by

$$\Gamma(\tau)e^{\tau d} = \Gamma(0) + [\Gamma'(0) + \Gamma(0)d]\tau + O(\tau^2). \quad (23)$$

Furthermore, by using symbolic mathematic tools, such as Mathcad®, to solve $\Gamma(\tau)$, one can easily verify that

$$\Gamma(0) \quad = \quad 1. \tag{24}$$

By preserving the first moment in Eq. 23, $\Gamma(\tau)e^{\tau d}$ can be approximated by constant one when

$$d \quad = \quad -\Gamma'(0). \tag{25}$$

Therefore the multilayer substrate can now be substituted by a single image filament below its corresponding physical filament with distance $d + 2h$, which is called the effective complex distance (ECD). It is easy to show that ECD is uniquely determined by the substrate process parameters and the extraction frequency. One can use Mathcad® to solve ECD when the substrate includes many layers.

III. Eddy-Current-Aware PEEC model: EPEEC

We have shown that the effect of a lossy multilayer substrate can be approximated by image conductors, given currents in those conductors are evenly distributed. However, due to skin and proximity effects at high frequencies, conductor segments have to be discretized into filaments so as to account for the non-uniform current distribution [23] as shown in Fig. 2.

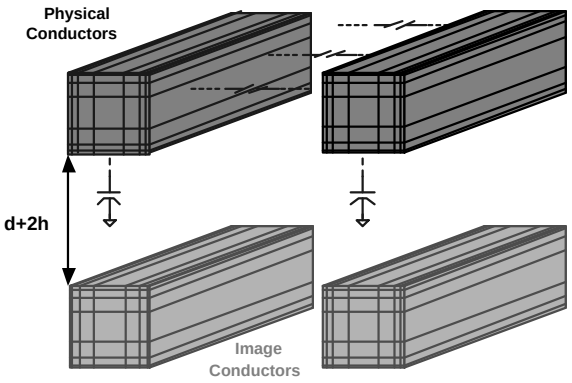

Fig. 2. Eddy-current-aware PEEC model. Each conductor is further discretized to consider the uneven distribution of currents.

In order to calculate the total inductance for a particular filament, it's necessary to combine its physical and image filaments together [24]. After applying complex image theory, the effective complex inductance (ECI) between filament i and j is given by

$$\mathcal{L}_{ij} \quad = \quad L_{ij} - L_{ij'}. \tag{26}$$

L_{ij} is the inductance between the physical filaments i and j and can be calculated by existing close-form static inductance formulas, such as Hoer's formula [25] and Grover's formula [26]. $L_{ij'}$ is the inductance between the physical filament i and the image filament j'.

Since the calculation of $L_{ij'}$ depends on ECD, so that $L_{ij'}$ will depend on frequency and substrate parameters. Hoer's formula can be accurately extended to calculate inductances of rectangular filaments separated by complex distances.

Notice that although applying complex image theory doubles the computational complexity, it will not increase the model size since $L_{ij'}$ is basically used to modify the value of L_{ij} after considering the lossy substrate effects.

The filament impedance matrix $\hat{Z}(\omega)$[1] at frequency $\omega/2\pi$ can be expressed as follows

$$\hat{Z}(\omega) \quad = \quad \hat{R}_{DC} + j\omega\hat{L}. \tag{27}$$

$\hat{L}$ is the filament inductance matrix containing $\mathcal{L}_{ij}$'s by using Eq. 26. $\hat{R}_{DC}$ is a diagonal matrix including DC resistances of physical filaments.

A. EPEEC Interconnect Modeling Algorithm

For a complicated interconnect system, the number of passive elements will be huge if inductance extraction is applied. Moreover, the discretization of conductors further increases the model size. We will show that complex image theory can be easily combined with reluctance extraction to generate compact interconnect models.

Most existing reluctance extraction tools are based on window selection algorithms [27], [28]. Here we propose an extended window selection algorithm to handle both physical conductors and their images.

BEGIN
For each conductor in the interconnect system
a. Applying a general window algorithm to select its neighboring physical conductors;
b. Once one physical conductor is selected as a neighboring conductor, its corresponding image is also selected.
END

TABLE I
Extended Window Selection Algorithm.

We illustrate the algorithm in Table I by a simple example shown in Fig. 3. If the current aggressor is conductor 1, its neighboring conductors include 3, 4, and 5. Therefore, their image conductors $1'$, $3'$, $4'$, and $5'$ are also included into the current neighboring group.

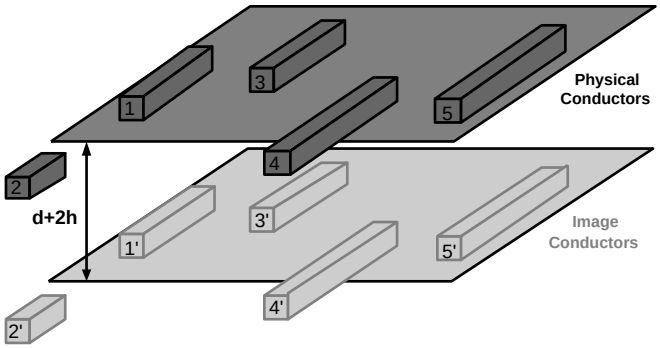

Fig. 3. Extended window selection algorithm to simultaneously consider physical and image conductors.

By using the extended window algorithm, we limit EPEEC to consider couplings within neighboring conductor groups

[1] A little hat ˆ is used to distinguish the symbols for filaments from those for conductor segments.

instead of the whole conductor system, and hence the computational complexity is significantly reduced.

For the neighboring group of conductor i, assume it contains n segments and the k^{th} conductor is discretized into p_k filaments, then the total number of filaments within the neighboring conductor group will be $n_f = \sum_{k=1}^{n} p_k$. Let $\hat{Z}_f^i(\omega) \in \mathbf{C}^{n_f \times n_f}$ denote the filament impedance matrix of this neighboring group with the consideration of substrate effects by using Eq. 27, then

$$\hat{Z}_f^i(\omega) \cdot \hat{I}_f^i \quad = \quad \hat{V}_f^i, \tag{28}$$

where $\hat{I}_f^i$, $\hat{V}_f^i \in \mathbf{C}^{n_f}$ are filament terminal current and voltage vectors, respectively.

Physically, a bundle of filaments within the same conductor segment can be treated as parallel branches. Merging parallel elements can be facilitated by using admittance instead of impedance. To directly calculate the admittance of each conductor segment, assume the current aggressor is conductor i, we simultaneously set voltages along all its p_i filaments to one while others in $\hat{V}_f^i$ to zero. The physical meaning of the current distribution $\hat{I}_f^i$ by solving Eq. 28 is that: the summation of all the filament currents within the aggressor is the aggressor admittance, while the summation of currents within one victim is the coupling admittance between the aggressor and that victim.

Those obtained admittance values are composed of two parts

$$y_{ij} \quad = \quad g_{ij} + jx_{ij}, \tag{29}$$

where g_{ij} is the conductance and x_{ij} is the susceptance. Obviously, if we model each conductor segment as serially connected resistance and reluctance, the equivalent resistance r_{ij} and reluctance k_{ij} can be synthesized as

$$\begin{aligned} r_{ij} &= \frac{g_{ij}}{g_{ij}^2 + x_{ij}^2}, \\ k_{ij} &= \frac{(g_{ij}^2 + x_{ij}^2)}{\omega x_{ij}}. \end{aligned} \tag{30}$$

The detailed EPEEC interconnect modeling algorithm is summarized in Table II.

INPUT: An interconnect system including n conductor segments; Extraction frequency f; Substrate parameters μ_k and σ_k.
OUTPUT: Resistance matrix R; Reluctance matrix K.
BEGIN I. Discretize all conductor segments according to their geometries and the extraction frequency f. II. For each conductor i in the interconnect system, do the following: **a.** Search its neighboring conductors Υ_i by adopting the extended window algorithm; **c.** Calculate the filament impedance matrix Z_f^i with the consideration of multilayer substrate effects by using Eq. 27; **d.** Set entries in the voltage vector V_f^i corresponding to filaments in conductor i to one while others to zero; **e.** Obtain the filament current distribution I_f^i by solving Eq. 28; **f.** The self admittance of conductor i equals the sum of filament currents within conductor i; the summation of filament currents in conductor j is the coupling between conductor i and j; **g.** Synthesize admittance into serial resistance and reluctance by applying Eq. 30. **f.** Stamp those values into parasitic matrices R and K respectively. **END**

TABLE II
EPEEC INTERCONNECT MODELING ALGORITHM.

B. SPICE Compatible Reluctance Realization

After constructing the resistance matrix R and the reluctance matrix K using the algorithm in Table II, circuit simulation is required to analyze those models. Unfortunately, traditional circuit analysis tools cannot handle reluctance directly. Although [7] and [28] incorporate the capability to simulate reluctance, significant modifications to traditional analysis tools are inevitable. In this subsection, we present a reluctance realization algorithm to directly convert reluctance to its mathematically and electrically equivalent circuit model, which only contains self inductances and voltage control voltage sources (VCVS) [29].

For a general circuit containing reluctances, the branch equation of self and mutual reluctances is given by

$$I_i = \sum_{j=1}^{n} K_{ij} V_j = K_{ii} V_i + \sum_{j=1, j \neq i}^{n} K_{ij} V_j \tag{31}$$

where K_{ii} is self reluctance and K_{ij} is the mutual reluctance between K_{ii} and K_{jj}. By rearranging the terms in Eq. 31, it can be written as:

$$V_i \quad = \quad \frac{1}{K_{ii}} I_i - \sum_{j=1, j \neq i}^{n} \frac{K_{ij}}{K_{ii}} V_j \tag{32}$$

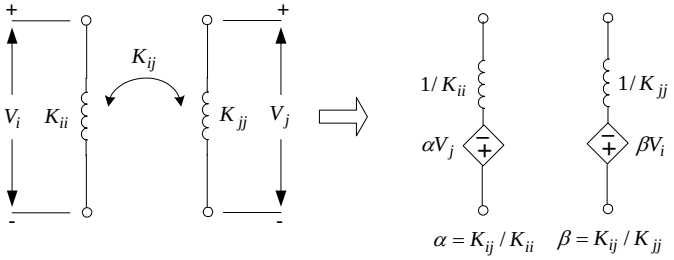

Fig. 4. SPICE compatible model for reluctance. The original reluctance element is substituted by serial self inductance and VCVSs.

If we take $1/K_{ii}$ as a self inductance, the original voltage drop across the self reluctance K_{ii} can be viewed as the combination of the voltage drops across that inductance and some VCVSs. These serial VCVSs are controlled by voltages on other self reluctances which are originally coupled with the reluctance K_{ii}. The gains of those VCVSs are determined by K_{ij}/K_{ii}.

Therefore, Eq. 32 can be used to construct the SPICE compatible model for reluctances shown in Fig. 4. The detailed reluctance realization algorithm is presented in Table III. It can be either combined into an extraction tool or programmed as a post-extraction software.

IV. EXPERIMENTAL RESULTS

Extensive experimental results are reported to show the efficiency and accuracy of our new interconnect modeling

BEGIN
For each reluctance K_{ii} between node n_i and n_j in a given circuit
a. q=0;
b. Let n_i^q=n_i;
c. For each self-reluctance K_{jj} that has mutual reluctance K_{ij} with self-reluctance K_{ii}:
Connect one VCVS controlled by V_j with gain $-K_{ij}/K_{ii}$ between n_i^q and n_i^{q+1};
q=q+1.
d. Connect inductance $1/K_{ii}$ between n_i^q and n_j.
END

TABLE III
RELUCTANCE REALIZATION ALGORITHM.

approach EPEEC. All tests are run on a Pentium IV $1.4GHz$ machine with $768MB$ memory.

A. EPEEC Model Validation

To validate the new modeling approach and to illustrate the accuracy, we first compare inductance and resistance values computed by complex image theory using Eq. 26 with FastHenry [23] and a more rigorous full-wave electromagnetic analysis tool, Sonnet®.

The experimental objects are two parallel conductor segments in a power/ground (P/G) network in metal layer 6. They are made of copper with conductivity $5.8 \times 10^7 S/m$. Both of them are $90\mu m$ long, $1.2\mu m$ thick, and $26\mu m$ wide. They are separated $60\mu m$ apart. The substrate is composed of two layers. The upper layer has conductivity $\sigma_1 = 100S/m$ while the lower layer conductivity $\sigma_2 = 10000S/m$. The thickness of the upper layer is $20\mu m$ and the lower layer $100\mu m$. The top area of the substrate is $1cm \times 1cm$. The distance between the substrate surface and the bottom of these conductors is $5.481\mu m$. Underneath the substrate, there is a ground plane. The detailed test configuration is shown in Fig. 5.

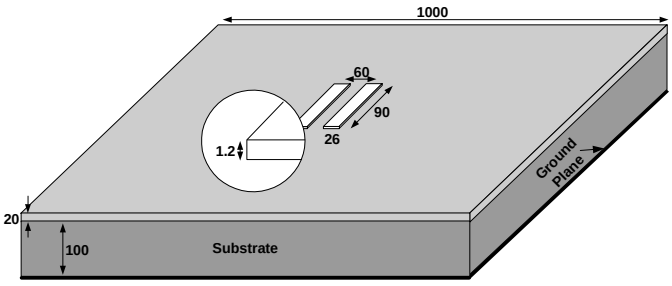

Fig. 5. Test configuration: two parallel copper interconnects above a two-layer substrate (Length unit: μm).

The self inductance of one wire is calculated and compared. Up to $20GHz$, EPEEC gives inductance values that are very close to full-wave simulation results (within 1.5% error) and shows over $100X$ speedup compared to FastHenry and Sonnet®.

B. Substrate Effects

As shown in Fig. 6, interconnect models are essentially frequency dependent. Besides frequency, many other factors

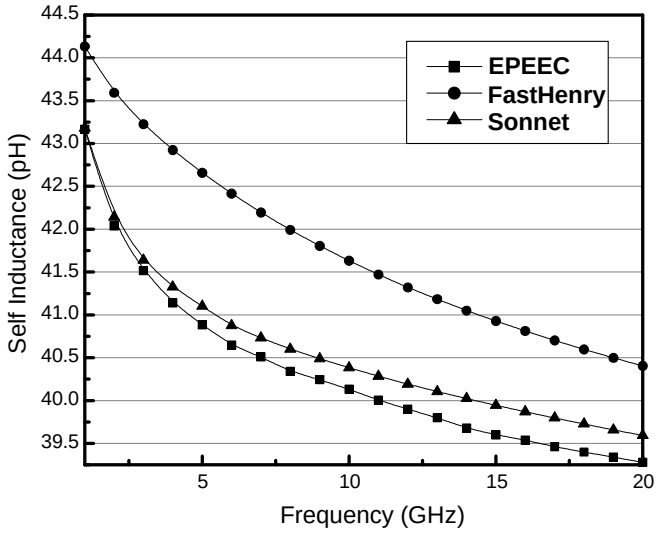

Fig. 6. Self inductance comparison by using three different extraction tools: FastHenry, Sonnet®, and EPEEC.

may also affect inductance and resistance values, such as conductor-substrate distance, substrate conductivity, and substrate thickness. The next set of experiments investigates how those factors can impact parasitic values.

In order to minimize the skin and proximity effects, we select two thin signal lines in metal layer 6. Both of them are $90\mu m$ long, $1.2\mu m$ thick, and $0.6\mu m$ wide. They are separated $1.2\mu m$ apart. The substrate has the same configuration as the above test. Without considering the substrate, i.e. in free space (PEEC), the self inductance and resistance are $91.95pH$ and 2.16Ω respectively.

First, we discuss the substrate effect under different frequencies and with different conductor-substrate distances. Figs. 7 and 8 show that the substrate effect becomes more evident under higher frequencies and when conductors are getting closer to the substrate. The increased inductive and ohmic substrate losses are expressed by smaller inductance and larger resistance values. At $10GHz$ and with conductor and substrate separated by $10\mu m$, the inductance value becomes $85.14pH$ which shows 8% deviation from the value calculated in free space.

Second, we show the impact of substrate conductivities of different layers. For a multilayer substrate in real design, the upper layer is usually less conductive in order to facilitate the functionality of the on-chip analog circuitry. Low conductivity prevents the generation of large eddy currents in the upper layer. However, since low conductivity medium has large skin depth, the electromagnetic field can easily penetrate through the upper layer to reach lower layers and hence lower layers may have more significant effects on interconnect values.

We set the conductor-substrate distance to $5.48\mu m$ at $10GHz$. To fairly compare two layers, they are both set to $50\mu m$ thick. From Fig. 9, one can see that the upper layer will have large impact compared to the lower layer when two layers have the same conductivity. However, if the upper layer conductivity is small, the low layer effect also cannot be ignored. When $\sigma 1 = 200S/m$, the upper layer has skin

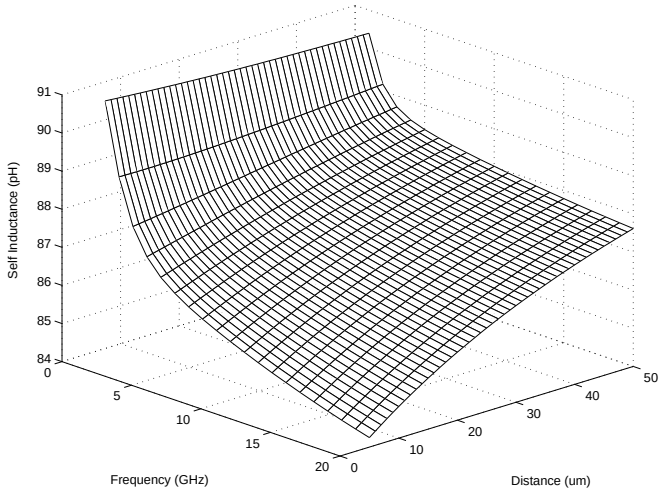

Fig. 7. Self inductance decreases as frequency increases and conductor-substrate distance decreases.

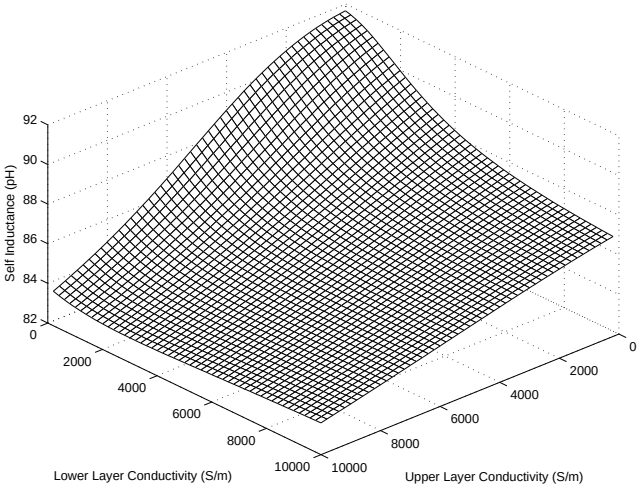

Fig. 9. With the same conductivity, the upper layer substrate will have larger effect than the lower layer. However, the lower layer cannot be ignored when the thickness of the upper layer is less than its skin depth.

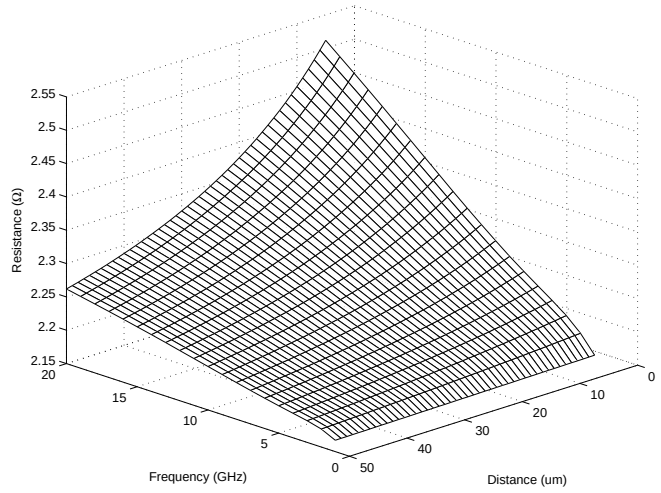

Fig. 8. Resistance increases as frequency increases and conductor-substrate distance decreases.

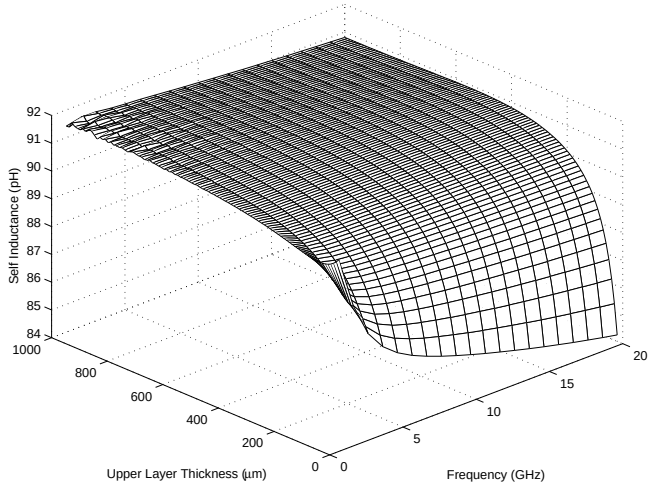

Fig. 10. Self inductance saturates when the thickness of the upper layer grows over its skin depth.

depth $355.88\mu m$ which is much larger than its thickness. In this scenario, if $\sigma 2 = 1000S/m$, the inductance value will be $91.45pH$. While changing $\sigma 2$ to $10000S/m$ gives the inductance value $87.05pH$, which is 5.1% different from the previous value.

Therefore, although the upper layer normally has low conductivity, it determines to what extent the lower layers affect interconnects. In the case that the upper layer thickness is smaller than its skin depth, one cannot simply discard the effects from lower layers. To proof this, we set the upper layer and the low layer conductivity to $100S/m$ and $10000S/m$ respectively, and then we gradually increase the upper layer thickness to see what will happen on line parameters.

From Figs. 10, one can see that at a specific frequency, when the upper layer thickness grows over its skin depth, increasing its thickness will not have further effects on interconnects. In this experiment, since the upper layer has low conductivity, when the interaction between interconnects and the low substrate layer is blocked by a thick upper layer, the overall substrate effect becomes insignificant.

C. Inductance vs. Reluctance

The next set of experiments is run to show the computational complexity and model size of EPEEC compared to PEEC. The testing conductor system includes 604 conductor segments which are in a P/G network located within metal layer 7 and 6. The substrate configuration is the same as previous tests.

As shown in Table IV, PEEC and EPEEC-L[2] have identical model size, while the extraction time of EPEEC-L is roughly doubled since we need to calculate inductances for both

[2]EPEEC-L means we apply complex image theory while extracting inductance. EPEEC-R is obtained by extracting reluctance using the algorithm given in Table II.

	Extraction Time	Number of Passive Elements
PEEC	38.162s	92,639
EPEEC-L	91.547s	92,639
EPEEC-R	4.094s	2,794

TABLE IV
EXTRACTION TIME AND MODEL SIZE COMPARISON.

physical and image conductors in Eq. 26. However, the model size and extraction time of the EPEEC-R is greatly reduced. For larger interconnect systems, the improvement will be even more significant.

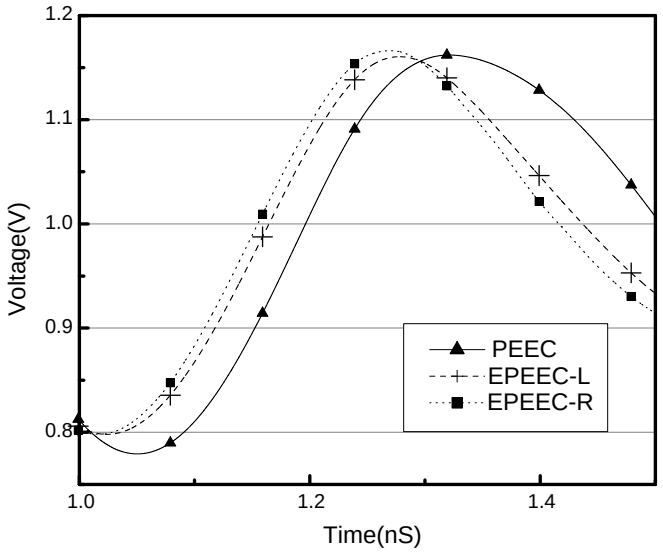

Fig. 11. Waveforms of transient responses by using different interconnect models: PEEC, EPEEC-L, and EPEEC-R.

Since substrate affects values of passive elements in the EPEEC model, it impacts the transient responses which are critical for timing and signal integrity analysis. To compare different responses at different frequencies by using PEEC, EPEEC-L, and EPEEC-R models, we randomly select one node in the above P/G network. Since PEEC model does not consider the substrate, it only depends on geometries of conductors and is frequency independent. However, at high frequencies, ignoring substrate will lead to significant errors in the transient response.

As shown in Fig. 11, at $20GHz$, the waveforms of PEEC and EPEEC-L exhibit about 10% difference, which is intolerable for the present interconnect modeling accuracy requirement. On the contrary, the reluctance model EPEEC-R demonstrates much smaller model size while maintaining less than 1.5% error compared to EPEEC-L.

V. CONCLUSION

This paper proposes an accurate and compact interconnect modeling approach EPEEC. EPEEC extends complex image theory to handle multilayer substrates and develops a reluctance-based extraction algorithm to consider inductive and ohmic losses due to induced eddy currents in a multilayer substrate. Furthermore, EPEEC is SPICE-compatible by employing a reluctance realization algorithm which converts one reluctance element to serial self inductance and VCVSs. Extensive experiments demonstrate that EPEEC has high accuracy and can generate very compact interconnect models.

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