INDUCTWISE: Inductance-Wise Interconnect Simulator and Extractor

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Abstract—A robust, efficient, and accurate inductance extraction and simulation tool, INDUCTWISE, is developed and described in this paper. This work advances the state-of-the-art inductance extraction and simulation techniques, and has several major contributions. First, albeit the great benefits of efficiency, the recently proposed inductance matrix sparsification algorithm, the K-method (Ji *et al.* 2001), has a flaw in the stability proof for general geometry. We provide a theoretical analysis as well as a provable stable algorithm for it. Second, a robust window-selection algorithm is presented for general geometry. Third, integrated with the nodal analysis formulation, INDUCTWISE achieves exceptional performance without frequency-dependent complex operations and directly gives time-domain responses. Experimental results show that INDUCTWISE extractor and simulator have dramatic speedup compared to FastHenry and SPICE3, respectively. It has been well tested and released on the web for public usage (Available: http://vlsi.ece.wisc.edu/Inductwise.htm).

Index Terms—Circuit simulation, inductance extraction, interconnect, on-chip parasitic modeling.

I. INTRODUCTION

PARASITIC on-chip inductance is growing as another design concern as the very large scale integration (VLSI) technology marches toward ultradeep submicron and the operation frequency approaches the gigahertz range. Inductive coupling effect becomes more important because of higher frequency signal content, denser geometries, and reductions of both resistance and capacitance by copper and low-K devices. Inductance effect is present not only in IC packages but also in on-chip interconnects such as power grids, clock nets, and bus structures. It causes signal overshoot, undershoot, and oscillations, and aggravates crosstalk and power-grid noises. All of these seriously impact the on-chip signal integrity. The importance and difficulty of on-chip inductance extraction and analysis have been addressed in [3] and [4].

One major problem of inductance modeling is the long range coupling effect and the uncertainty of return paths. Since inductance is a function of a closed loop, the return path is difficult to predict in advance before simulation. For this reason, A. Ruehli

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developed the famous partial element equivalent circuit (PEEC) method [5] model, which defines the partial self and mutual inductances with the assumption of infinite return paths. FastHenry [6] utilizes a multipole acceleration technique to speed up the extraction process in the frequency domain. Chang *et al.* [7] proposed to directly simulate the PEEC model in the time domain so as to determine the return paths. This method has been shown to be accurate in a wide range of frequencies. Another fast simulation method [8] based on the precorrected-FFT method [9] has been published recently.

The PEEC model, however, leads to a large-scale dense inductance matrix due to the long-range effect of inductive coupling and the uncertainty of current return. Traditional circuit simulation engines may require hours or even days for solving such a large-scale dense matrix. To effectively reduce the mutual inductance terms, sparsification is crucial. It has been shown that direct truncation of the inductance matrix could result in instability [10]. Thus, a provable stable shift-and-truncate method was proposed by Krauter *et al.* [11]. This method assumes that the return path is no longer at infinity, but within a shell. Other methods such as the Halo method [12] and the block diagonal method [13] also reduce the number of mutual inductances by limiting the return path to the nearest power and ground returns. Later, Beattie and Pileggi [14] develops an exponential shell return paths for further sparsfication and shows that the reachable sparsity is close to that of the K-method mentioned below.

Recently, the K-method has been presented by Hao Ji *et al.* [1], [15]. K is the inverse of the partial inductance matrix L. Since K has a higher degree of locality similar to capacitance, it is more satisfactory to sparsify K than L. Furthermore, [15] also shows that the K matrix is diagonally dominant, and hence, positive definite. The off-diagonal terms are negative and can be safely deleted without sacrificing stability. Later, Beattie and Pileggi [14] also proposed to do double inversion on the inductance matrix and perform sparsification on both inductance and susceptance matrices.

Most of the existing works [1], [14]–[16] discussed equal-length conductors to show the benefits of sparsification on inverse-inductance matrices. The accuracy and stability of the inverse-inductance matrix-sparsification method have not yet been revealed when the targeting circuit has irregular geometry. In this paper, we propose an efficient, accurate, and inductance-wise interconnect simulator and extractor, INDUCTWISE, which is based on the inverse-inductance (named reluctance) method. We explore the reluctance method for general geometry cases and discover that the proof for the stability of the original K-method sometimes fails for some irregular cases. With a

counterexample, theoretical study, and proof, we are able to develop an auxiliary algorithm to avoid these cases. An additional window selection algorithm presented also makes the reluctance method feasible to general circuit cases and full-chip reluctance extraction applicable. Moreover, utilizing the nodal analysis formulation and the Cholesky decomposition allows our INDUCTWISE to directly take reluctance elements into simulation, which demonstrates tremendous efficiency.

The organization of this paper is as follows. Section II presents several issues and solutions of the INDUCTANCE extractor. Section III introduces the methodology of the INDUCTANCE simulator. Simulation results and the conclusion are given in Section IV.

II. INDUCTWISE EXTRACTOR

In this section, the INDUCTWISE extractor is proposed. First, we introduce the inductance and reluctance matrices and the K-method. Then, we show that the proof of stability of the K-method does not hold for general cases, and provide a remedy algorithm called recursive bisection algorithm (RBA). Later, we present a novel window selection algorithm (WSA) that enables our extractor to extract the reluctance elements in any circuit configuration.

A. Inductance and Reluctance Matrices

Given an inductance matrix $\mathcal{L}$, the K-matrix is defined as $\mathcal{K} = \mathcal{L}^{-1}$ [15]. Beattie and Pileggi [14] name it susceptance. However, susceptance is a general term for the imaginary part of admittance that can be caused by capacitance or inductance. Since the definition of reluctance is *the ratio of the total current force to the total magnetic flux in a magnetic circuit or component* and its unit is reciprocal Henry (H^{-1}), we think that the *reluctance matrix* is more specific to the inverse inductance matrix $\mathcal{K}$.

Each element in the partial inductance matrix is given by

$$\mathcal{L}_{ij} = \frac{\mu_0}{4\pi a_i a_j} \left[\int_{a_i} \int_{a_j} \int_{l_i} \int_{l_j} \frac{dl_i \cdot dl_j}{r_{ij}} da_i da_j \right] \quad (1)$$

where a_i and a_j are cross-sections of segments i and j, respectively, and r_{ij} is the geometric distance between two points in segments i and j. For an $n \times n$ partial inductance matrix, the corresponding linear system equation can be written as follows:

$$\begin{bmatrix} \mathcal{L}_{11} & \mathcal{L}_{12} & \cdots \\ \mathcal{L}_{21} & \mathcal{L}_{22} & \cdots \\ \cdots & \cdots & \mathcal{L}_{nn} \end{bmatrix} \begin{bmatrix} I_1 \\ \vdots \\ I_n \end{bmatrix} = \begin{bmatrix} \Phi_1 \\ \vdots \\ \Phi_n \end{bmatrix} \quad (2)$$

where I_j, $j = 1 \sim n$, is the current running along conductor segment j, and Φ_j is the total flux flowing through the virtual loop from segment j to infinity. Representing the system equation with $\mathcal{K}$, we get

$$\begin{bmatrix} \mathcal{K}_{11} & \mathcal{K}_{12} & \cdots \\ \mathcal{K}_{21} & \mathcal{K}_{22} & \cdots \\ \cdots & \cdots & \mathcal{K}_{nn} \end{bmatrix} \begin{bmatrix} \Phi_1 \\ \vdots \\ \Phi_n \end{bmatrix} = \begin{bmatrix} I_1 \\ \vdots \\ I_n \end{bmatrix}. \quad (3)$$
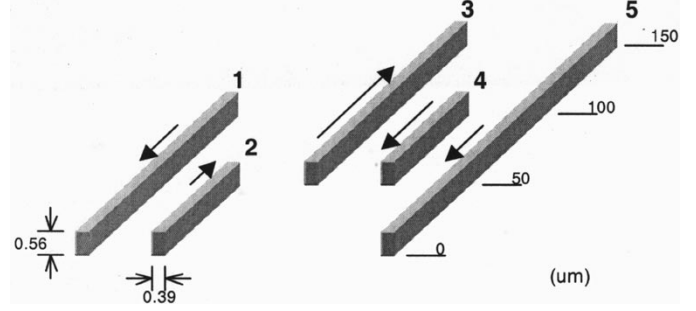

Fig. 1. Example of parallel conductors with unequal lengths.

B. Stability Issues of the K-Method

H. Ji *et al.* [1] developed an advanced reluctance sparsification method called K-method. They showed that $\mathcal{K}$ has better locality than $\mathcal{L}$, and thus, to sparsify $\mathcal{K}$ actually benefits more efficiency. They proved the stability of the algorithm based on the diagonal dominance property, which is derived from the assumption that all off-diagonal terms of $\mathcal{K}$ are negative. We now show that this property does not hold for general geometry.

From (3), the physical meaning of $\mathcal{K}_{ij}$ is defined by the induced current along the ith conductor when the total flux for the jth conductor is equal to one and those for all other conductors are set to zero. For example, as shown in Fig. 1, to get the third row of $\mathcal{K}$, we apply unit flux to conductor 3 and zero to all the others. The induced currents on conductors other than the third are the off-diagonal terms in the third row of $\mathcal{K}$. It is positive if the current direction and the applied flux direction follow the right-hand rule; it is negative otherwise. Devgan and Dai [1] argue that all of the induced currents are negative and uses this property to prove the stability of their algorithm. We find out that the off-diagonal terms are not necessarily negative for general cases.

In this example, the partial inductance matrix is calculated as follows:

$$\mathcal{L} = \begin{bmatrix} 1.04 & 0.34 & 0.37 & 0.24 & 0.51 \\ 0.34 & 0.45 & 0.09 & 0.06 & 0.27 \\ 0.37 & 0.09 & 1.04 & 0.34 & 0.41 \\ 0.24 & 0.06 & 0.34 & 0.45 & 0.11 \\ 0.51 & 0.27 & 0.41 & 0.11 & 1.69 \end{bmatrix} \times 10^{-10} H. \quad (4)$$

By inverting $\mathcal{L}$, the $\mathcal{K}$ matrix is obtained

$$\mathcal{K} = \begin{bmatrix} 1.57 & -0.94 & -0.22 & -0.47 & -0.25 \\ -0.94 & 3.02 & 0.15 & 0.01 & -0.23 \\ -0.22 & 0.15 & 1.42 & -0.93 & -0.24 \\ -0.47 & 0.01 & -0.93 & 3.12 & 0.16 \\ -0.25 & -0.23 & -0.24 & 0.16 & 0.75 \end{bmatrix} \times 10^{10} H^{-1}. \quad (5)$$

It is clear that some off-diagonal terms in (5) are positive. For instance, when calculating the third row, a unit flux is assigned on conductor 3, which demands positive current along conductor 3 to accomplish. This current induces positive magnetic flux along all other conductors (consider only conductors 1 and 2 in this explanation). To compensate this effect and to make the net magnetic flux along 1 and 2 equal to zero, they have to carry negative current. However, the induced current along 1 also induces another current along 2. Since the coupling effect

between 1 and 2 is much stronger than that between 3 and 2, the overall effect causes conductor 2 to carry a positive current direction.

Therefore, the physical definition of $\mathcal{K}$ in [1] should be revised as follows. *When calculating the self and mutual reluctances for conductor j, we set a unit magnetic flux for the jth conductor, and zero flux for all others. There exists a current combination such that the overall magnetic effect satisfies the configuration. The reluctance element $\mathcal{K}_{ij}$ is then the current flowing through the ith conductor.* Since the result is due to the overall effect (not a single active line), negative off-diagonal elements are not guaranteed anymore. This invalidates the proof of the diagonal dominance property, and hence, the stability of the K-method becomes questionable. We will provide a solution for this problem in the next section.

C. Formal Analysis

In this section, we present stability analysis of the K-method by the duality of electric and magnetic fields, then throw some light on the similarity between inductance and capacitance problems. Through the theorem provided in this section, we propose a correction to the K-method to ensure the stability.

From the Maxwell's equations, we have

$$\nabla \times \vec{E} = -\mu s \vec{H} \tag{6}$$

$$\nabla \times \vec{H} = \epsilon s \vec{E} + \vec{J} \tag{7}$$

$$\nabla \cdot \epsilon \vec{E} = \rho \tag{8}$$

$$\nabla \cdot \mu \vec{H} = 0. \tag{9}$$

The definition of the magnetic vector potential gives

$$\mu \vec{H} = \nabla \times \vec{A}. \tag{10}$$

Applying (10) to (6), we get

$$\nabla \times (\vec{E} + s\vec{A}) = 0. \tag{11}$$

This implies that there exists a scalar potential V such that

$$\vec{E} + s\vec{A} = -\nabla V. \tag{12}$$

To uniquely determine $\vec{A}$, we choose the Lorentz gauge

$$\nabla \cdot \vec{A} = -\epsilon \mu s V. \tag{13}$$

By (7), (10), and (13) and the identity $\nabla \times (\nabla \times \vec{A}) = \nabla(\nabla \cdot \vec{A}) - \nabla^2 \vec{A}$, we get

$$\nabla^2 \vec{A} - \mu \epsilon s^2 \vec{A} = -\mu \vec{J}. \tag{14}$$

Similarly, by (8), (11) and the Coulomb gauge, we get

$$\nabla^2 V - \mu \epsilon s^2 V = -\frac{\rho}{\epsilon}. \tag{15}$$

Equations (14) and (15) are often referred to as the **nonhomogeneous Helmholtz's equations**. The solutions of (14) and (15) are

$$\vec{A}(r) = \frac{\mu}{4\pi} \int_{V'} G(r, r') \vec{J}(r') e^{\frac{s}{c}|r-r'|} dv' \tag{16}$$

$$V(r) = \frac{1}{4\pi\epsilon} \int_{V'} G(r, r') \rho(r') e^{\frac{s}{c}|r-r'|} dv' \tag{17}$$

in which V' is the volume of all conductors, $c = 1/\sqrt{\mu\epsilon}$, and $G(r, r') = (1/4\pi R_{ij})$, where $R_{ij} = |r - r'|$ is the Green's
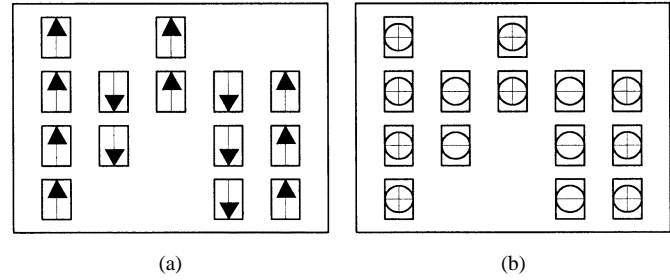

Fig. 2. Dual property between inductance and capacitance problems. (a) Inductance model. (b) Capacitance model.

function. The dual property between a magnetic problem and an electric one can be observed from (14)–(17). The major difference between $\vec{A}$ and V is that $\vec{A}$ is a directional vector and V is a scalar. There exists a transformation between a magnetic problem and an electric problem, which is described in the following lemma.

Lemma 1: Given a unidirectional magnetic nonhomogeneous Helmholtz's equation problem, there exists a corresponding electric nonhomogeneous Helmholtz's equation problem that has the same solution.

Proof: Since all of the magnetic sources and mediums are unidirectional, we can remove the vector natural by properly assigning the positive charge corresponding to the forward direction, or negative otherwise. Hence, given a current source vector $\vec{J}$, we can create a corresponding charge $\rho = \mu\epsilon\vec{J}$ with a proper sign assigned, and then the solution of (14) and (15) are identical. ∎

Fig. 2 illustrates the transformation between inductance and capacitance problems in Lemma 1. From this lemma, we have the following theorem.

Theorem 1: The reluctance matrix $\mathcal{K}$ is diagonally dominant and symmetric positive definite when all the conductors are sufficiently discretized.

Proof: Lemma 1 shows that every unidirectional magnetic problem can be transformed into an electric one. Since it has been shown that the capacitance matrix is always diagonally dominant and symmetric positive definite for sufficiently discretized problem [5], Theorem 1, thus, follows. ∎

Theorem 1 reveals why the diagonal dominance property of the reluctance matrix does not always hold. The answer is **discretization**. When we perform capacitance extraction, conductors are usually well discretized. On the contrary, conductors are often preserved as long wires while we perform inductance extraction. The length of inductance discretization is generally a hundred times larger than the capacitance discretization.

Performing finer discretization, the circuit in Fig. 1 becomes the one in Fig. 3. The corresponding $\mathcal{K}$ switches from (5) to the following one, whose off-diagonal elements are all nonpositive (see equation at bottom of the next page).

In this example, we uniformly cut all segments into smaller ones. For efficiency's sake, we do not have to examine all the positive off-diagonal elements in the *dense* $\mathcal{K}$ and discretize conductors this fine. What we have to do is to perform bisection only when positive off-diagonal elements occur in the *sparse* $\mathcal{K}$. Therefore, we come up with the RBA in the following subsection.
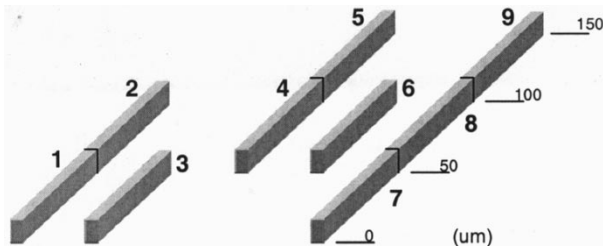
Fig. 3. Finer discretization example.

D. RBA: Guarantee the Stability

We have already shown that finer discretization guarantees the stability of the K-method. It can also improve the accuracy. However, if we uniformly discretize conductors into small pieces, the complexity of solving this problem will become enormous and the original intention of the sparsification is lost. Therefore, we propose a cutting algorithm to obtain a stable reluctance matrix without increasing the simulation time too much. RBA is based on the idea that the reluctance matrix is diagonally dominant and symmetric positive definite (SPD) when the conductors are sufficiently discretized.

From the previous discussion, the positive off-diagonal terms of $\mathcal{K}$ are strongly related to unequal-length and misalignment cases. According to Theorem 1, finer discretization is better than coarser ones, which implies that the longest conductor actually plays a critical role in this problem. Thus, the basic idea of the RBA is to recursively cut the longest conductor when positive off-diagonal elements occur during the K-method procedure. In order to make sure that the RBA results in all nonpositive off-diagonal elements in $\mathcal{K}$, we perform the K-method with a small window (we will discuss how to choose the window in the following section) and check if every off-diagonal element in the small K-matrix is nonpositive. If there exists any positive off-diagonal term, we cut the longest conductor in this window. After this cutting, back-trace those conductors that are reluctance-coupled with the bisected one. If any positive off-diagonal value remains in the system or the cutting causes new positive off-diagonal terms, we recursively cut the troublemaker conductors and repeat this procedure until the final K-matrix has all nonpositive off-diagonal entries. The RBA is summarized in Table I.

Theorem 2: The RBA guarantees that all off-diagonal elements in $\mathcal{K}$ are nonpositive, and hence, the SPD property validates the proof of stability in [1].

TABLE I
RBA

Input: Given a parallel-conductor system

For each conductor j
1. Choose a window W.
2. Calculate $\mathcal{K}_{ij}$, where $i \in W$ by setting a unit flux on conductor i and zero to others.
3. If $\exists \mathcal{K}_{ij} > 0$, $i \in W$ and $i \neq j$, do the following:
   a. Cut the longest conductor l, $l \in W$, by half.
   b. Back-trace and redo Steps 1 and 2 for the kth conductor, where $k \in W$ and $k < j$. If this cutting causes any new positive off-diagonal term, recursively perform the cutting on the troublemaker conductor.

Proof: The RBA recursively checks the off-diagonal values during the extraction process. Thus, Theorem 2 follows by Theorem 1 and the recursion. ∎

We have already known that positive off-diagonal values occur when conductors have seriously mismatched lengths or misaligned organizations. Since all previous works [1], [14], [16] considered only equal-length parallel conductors, the exception case that we showed does not exist in previous works. However, to build a full-chip inductance (reluctance) extractor, this possibility does exist. We propose this cutting algorithm serving as the stability guard of our INDUCTWISE extractor to ensure our sparse reluctance matrices SPD. In the following section, we will show how to select the window for general geometries.

E. WSA: Capture the Significant Effect

Most of the existing works [1], [14]–[16] discussed equal-length conductors to show the benefits of sparsifying reluctance matrices. It is not clear if the K-method can work on general irregular geometries. The lack of generality limits the application of the K-method only to the analysis of some special configurations such as buses. However, general routing cases are more irregular, which might contain uneven-length or misaligned conductors. For these cases, it is very difficult to determine what a "window" is when performing the window-based K-method. In this section, we propose a novel algorithm to determine what should be included in the window when we extract sparse reluctance matrices. Let us first define the terminology used in the following discussion by the example circuit in Fig. 4.

$$\mathcal{K} = \begin{bmatrix} 2.33 & -0.14 & -2.01 & -0.05 & -0.02 & -0.03 & -0.39 & -0.05 & -0.02 \\ -0.14 & 2.96 & -0.08 & -1.01 & -0.13 & -0.31 & -0.07 & -0.27 & -0.09 \\ -2.01 & -0.08 & 2.63 & -0.07 & -0.02 & -0.04 & -0.76 & -0.05 & -0.02 \\ -0.05 & -1.01 & -0.07 & 3.98 & -0.11 & -1.73 & -0.06 & -0.43 & -0.05 \\ -0.02 & -0.13 & -0.02 & -0.11 & 2.76 & -0.06 & -0.03 & -0.07 & -1.30 \\ -0.03 & -0.31 & -0.04 & -1.73 & -0.06 & 3.63 & -0.07 & -1.81 & -0.07 \\ -0.39 & -0.07 & -0.76 & -0.06 & -0.03 & -0.07 & 3.65 & -0.15 & -0.03 \\ -0.05 & -0.27 & -0.05 & -0.43 & -0.07 & -1.81 & -0.15 & 3.78 & -0.15 \\ -0.02 & -0.09 & -0.02 & -0.05 & -1.30 & -0.07 & -0.03 & -0.15 & 1.82 \end{bmatrix} \times 10^{10} H^{-1}.$$
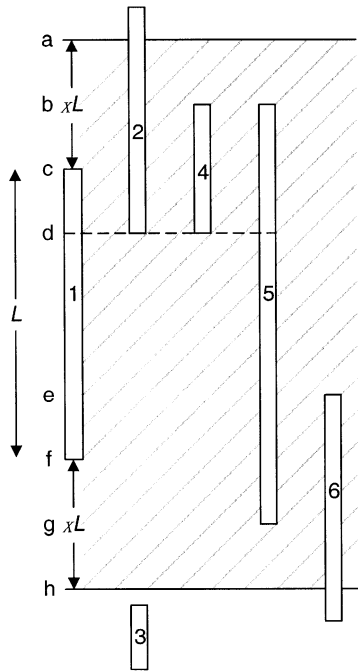
Fig. 4.   Circuit example for the definition of shielding.

TABLE II
WSA

Input:	Given ESF= x, shielding level= k, and a conductor system

1. Divide all conductors into vertical and horizontal sets.
2. Sort the vertical set by their x coordinates.
3. For every conductor from left to right, do the following:
   a. Search from the first victims right next to the aggressor, and select those shields (by definition) until every segment on the ESR (i.e. $\overline{ah}$ in Fig.4.) is shielded no less than k levels. This forms the right part of the window.
   b. The left part of the window is obtained from the window-selection results of previous conductors.
   c. Set the flux along the aggressor to one and others to zero, and solve the reluctance elements by calculating the induced currents in the selected window. The resulting elements form the column of $\mathcal{K}_{asym}$ that corresponds to the aggressor.
4. Following the same analogy, repeat steps 2 and 3 for the horizontal set.
5. Symmetrize by $\mathcal{K} = \frac{1}{2}(\mathcal{K}_{asym} + \mathcal{K}_{asym}^T)$.

- **Aggressors and Victims**: When performing the K-method and calculating one of the columns in $\mathcal{K}$, we set the magnetic flux along the corresponding conductor to one called the **aggressor**, and others to zero called **victims**. In Fig. 4, we assume that conductor 1 is now the aggressor and all others are victims.
- **ESF, ESR, and ESA**: Suppose the aggressor has length L. We define the **extended search factor (ESF)** x such that the **effective search range (ESR)** increases from the length of the aggressor L (i.e., segment $\overline{cf}$) to $(1+2x)L$ (i.e., segment $\overline{ah}$). Then, the **effective search area (ESA)** is defined by sweeping from left infinity to right infinity with the ESR. The ESA is marked by slash lines in Fig. 4.
- **Shields and Shielding Level**: If a victim is partially or fully in the ESA, it is called a **shield** for the aggressor. For example, in Fig. 4 conductors 2, 4, 5, and 6 are shields of 1, but 3 is not. The **shielding level** indicates how close the victim shields the aggressor. If there exist k shields between a shield and the aggressor, the shield is of the $(k+1)$th level. For example, conductor 2 is the shield of the first level for segment $\overline{ad}$, and conductor 4 is the shield of the second level for $\overline{bd}$. Conductor 5 contains two part. The upper part is the shield of the third level for $\overline{bd}$ and the lower part is the shield of the first level for $\overline{dg}$.

We now discuss how and why the K-method works from both the physical and numerical points of view. From the physical point of view, the experiment results in [1] demonstrate that the shielding effect of the mutual reluctance does exist but not for partial mutual inductance. It means a conductor that is shielded by any other conductor is more likely to be excluded from the reluctance extraction window. From the numerical point of view,

the K-method tries to select the most significant values on a column (row) and inverts the small matrix in the window. The inversion causes the off-diagonal values of $\mathcal{K}$ to decrease faster than $\mathcal{L}$. This fact makes the reluctance element have better locality than the partial inductance. Therefore, selecting relatively significant couplings within the small window properly dominates the accuracy of the algorithm.

However, the K-method encounters some difficulties for irregular geometries. First, the strength of coupling does not strictly decrease as their distances increase, so the closer one may not be the more significant one. This means that a farther conductor may have stronger coupling but is not included in the window. Second, an intuitional solution is to select the largest inductive coupling values in the small window. To find the largest off-diagonal entries in the corresponding column of $\mathcal{L}$, we have to extract all the partial mutual inductance values, which makes the extraction complexity $O(n^2)$ and loses the efficiency and the intention of the sparsification. Moreover, this solution leads to a topologically asymmetric K-matrix and the later-on symmetrization process introduces more errors to the final sparse matrix $\mathcal{K}$.

In (1), the inner product of $dl_i \cdot dl_j$ implies that the mutual inductance has a large value when two conductors are parallel and next to each other, and has a small value when they are misaligned. If two conductors are perpendicular, their partial mutual inductance is zero. From these observations and utilizing the shielding effect of reluctance elements, given the ESF x and the desired shielding level k, which conductors should be included in the small window is determined by the window selection algorithm (WSA) that is summarized in Table II.

Note that we select the shields until every segment on the ESR is shielded no less than k levels to ensure that the significant effect is captured. For example, if we set the level of shielding to 1 in Fig. 4, the victims selected should be conductors 2, 5, and 6. Thus, all points on $\overline{ah}$ are shielded at least once. In this algorithm, we only have to search the right-hand side shields for each aggressor. The left-hand side shields can be obtained from the previous results, which can save half of the extraction time. The obtained K-matrix is topologically symmetric.
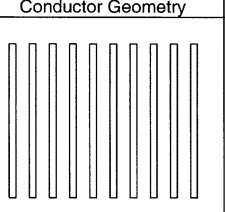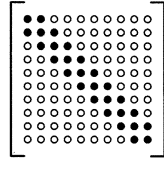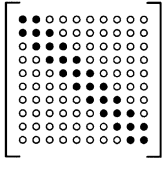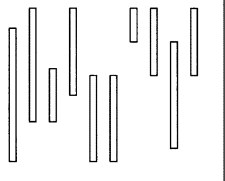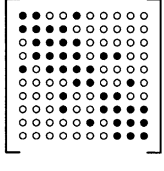
Fig. 5. Comparison between prior works and our WSA-based K-method.

Fig. 5 illustrates the difference between prior works and our WSA-based K-method. In this example, we set the desired shielding level to 1 and the ESF to 0. For equal-length cases, the WSA functions exactly the same as the original K-method does. For unequal-length and misaligned cases, the WSA can capture the important coupling values while prior works leave the problem undefined.

III. INDUCTWISE SIMULATOR

In this section, we present our efficient time domain RLKC INDUCTWISE simulator. We will first focus on two circuit matrix formulations MNA (modified nodal analysis) and NA (nodal analysis). Later, the way to deal with independent sources in the NA formulation and the pros and cons of these two formulations will be discussed.

A. MNA Approach

First, we briefly review the MNA equations. Given a linear circuit, the adjacency matrix, $\mathbf{A}$, can be determined from the directed graph by the following rule:

$$
\mathbf{A}_{ij} = \begin{cases} +1, & \text{if node } j \text{ is the source of branch } i \\ -1, & \text{if node } j \text{ is the sink of branch } i \\ 0, & \text{otherwise.} \end{cases}
$$

This matrix represents the connectivity of a circuit, and the Kirchhoff's law in terms of it is as follows:

$$
\text{KCL}: \mathbf{A}^T \mathbf{i}_b = \mathbf{0} \quad \text{and} \quad \text{KVL}: \mathbf{A} \mathbf{v}_n = \mathbf{v}_b \quad (18)
$$

where $\mathbf{i}_b$ and $\mathbf{v}_b$ are the vectors of branch currents and voltages, respectively, and $\mathbf{v}_n$ is the vector of the node voltages. For a circuit with RLC elements and current sources, the adjacency matrix, the branch voltages, and the branch currents can be partitioned into these forms

$$
\mathbf{A} = \begin{bmatrix} \mathbf{A}_s \\ \mathbf{A}_g \\ \mathbf{A}_c \\ \mathbf{A}_l \end{bmatrix} \quad \mathbf{v}_b = \begin{bmatrix} \mathbf{v}_s \\ \mathbf{v}_g \\ \mathbf{v}_c \\ \mathbf{v}_l \end{bmatrix} \quad \mathbf{i}_b = \begin{bmatrix} \mathbf{i}_s \\ \mathbf{i}_g \\ \mathbf{i}_c \\ \mathbf{i}_l \end{bmatrix}.
$$

The subscripts s, g, c, and l stand for branches, which contain independent current sources, resistors, capacitors, and inductors,

respectively. The relationships between branch currents and voltages are as follows:

$$
\mathbf{i}_s = -\mathbf{I}_s(t), \ \mathbf{i}_g = \mathcal{G}\mathbf{v}_g, \ \mathbf{i}_c = \mathcal{C}\frac{d}{dt}\mathbf{v}_c, \ \mathbf{v}_l = \mathcal{L}\frac{d}{dt}\mathbf{i}_l. \quad (19)
$$

$\mathbf{I}_s(t)$ is the vector of current sources. The conductance matrix $\mathcal{G}$ and capacitance matrix $\mathcal{C}$ are diagonal matrices. Implementing the traditional partial inductance extraction, the inductance matrix $\mathcal{L}$ turns out a dense matrix, which is known to be SPD.

MNA combines (18) and (19) and eliminates unnecessary branch currents except those running through inductors. Then we obtain the following:

$$
\tilde{\mathbf{G}}\mathbf{x} + \tilde{\mathbf{C}}\dot{\mathbf{x}} = \mathbf{b} \quad (20)
$$

in which

$$
\tilde{\mathbf{G}} = \begin{bmatrix} \mathbf{G} & \mathbf{A}_l^T \\ -\mathbf{A}_l & \mathbf{0} \end{bmatrix}
$$

$$
\mathbf{x} = \begin{bmatrix} \mathbf{v}_n \\ \mathbf{i}_l \end{bmatrix}
$$

$$
\tilde{\mathbf{C}} = \begin{bmatrix} \mathbf{C} & \mathbf{0} \\ \mathbf{0} & \mathcal{L} \end{bmatrix}
$$

$$
\mathbf{b} = \begin{bmatrix} -\mathbf{A}_s^T\mathbf{I}_s \\ \mathbf{0} \end{bmatrix}. \quad (21)
$$

In (21), $\mathbf{G} = \mathbf{A}_g^T\mathcal{G}\mathbf{A}_g$ and $\mathbf{C} = \mathbf{A}_c^T\mathcal{C}\mathbf{A}_c$, which are both SPD. For transient analysis, the trapezoidal integration approximation of (20) over the time interval $[kh, (k+1)h]$ is given by

$$
\tilde{\mathbf{G}}\left(\frac{\mathbf{x}^{k+1} + \mathbf{x}^k}{2}\right) + \tilde{\mathbf{C}}\left(\frac{\mathbf{x}^{k+1} - \mathbf{x}^k}{h}\right) = \frac{\mathbf{b}^{k+1} + \mathbf{b}^k}{2}.
$$

It can be rewritten as follows:

$$
\left(\tilde{\mathbf{G}} + \frac{2}{h}\tilde{\mathbf{C}}\right)\mathbf{x}^{k+1} = \left(-\tilde{\mathbf{G}} + \frac{2}{h}\tilde{\mathbf{C}}\right)\mathbf{x}^k + \mathbf{b}^{k+1} + \mathbf{b}^k. \quad (22)
$$

The MNA approach works for ordinary sparse partial inductance approximations, but not for the reluctance matrix. In this paper, we use this method to solve the exact solution with full $\mathcal{L}$ extraction.

B. NA Approach

Although the MNA provides a good solution for general circuits, the introduction of extra current variables makes the system matrix $(\tilde{\mathbf{G}} + (2/h)\tilde{\mathbf{C}})$ in (22) asymmetric, which makes the well-known Cholesky decomposition inapplicable. In this section, we will show that the NA is feasible for sparse reluctance matrices, and has even more advantages than the MNA method.

By substituting (21) for (22) and performing block matrix operations, we obtain two equations as follows:

$$
\left(\mathbf{G} + \frac{2}{h}\mathbf{C}\right)\mathbf{v}_n^{k+1} + \mathbf{A}_l^T\mathbf{i}_l^{k+1} = \left(-\mathbf{G} + \frac{2}{h}\mathbf{C}\right)\mathbf{v}_n^k + \mathbf{A}_l^T\mathbf{i}_l^k
$$
$$
- \mathbf{A}_i^T\left(\mathbf{I}_s^{k+1} + \mathbf{I}_s^k\right) \quad (23)
$$

$$
-\mathbf{A}_l\mathbf{v}_n^{k+1} + \frac{2}{h}\mathcal{L}\mathbf{i}_l^{k+1} = \mathbf{A}_l\mathbf{v}_n^k + \frac{2}{h}\mathcal{L}\mathbf{i}_l^k. \quad (24)
$$

Since $\mathcal{L}$ is positive definite and, thus, invertible, we multiply $(h/2)\mathcal{L}^{-1}$ to both sides of (24). Rearranging the terms, we get

$$
\mathbf{i}_l^{k+1} = \frac{h}{2}\mathcal{L}^{-1}\mathbf{A}_l\left(\mathbf{v}_n^{k+1} + \mathbf{v}_n^k\right) + \mathbf{i}_l^k. \quad (25)
$$

By substituting (25) for (23) and multiplying $2\mathbf{A}_l^T$ to both sides of (25), we get the following two equations:

$$\left(\mathbf{G}+\frac{2}{h}\mathbf{C}+\frac{h}{2}\mathbf{K}\right)\mathbf{v}_n^{k+1} = \left(-\mathbf{G}+\frac{2}{h}\mathbf{C}-\frac{h}{2}\mathbf{K}\right)\mathbf{v}_n^k$$
$$-2\mathbf{A}_l^T\mathbf{i}_l^k-\mathbf{A}_s^T\left(\mathbf{I}_s^{k+1}+\mathbf{I}_s^k\right) \quad (26)$$
$$2\mathbf{A}_l^T\mathbf{i}_l^{k+1} = h\mathbf{K}\left(\mathbf{v}_n^{k+1}+\mathbf{v}_n^k\right)+2\mathbf{A}_l^T\mathbf{i}_l^k \quad (27)$$

in which $\mathbf{K}=\mathbf{A}_l^T\mathcal{K}\mathbf{A}_l$, where $\mathcal{K}$ is the reluctance matrix that equals $\mathcal{L}^{-1}$. Let $\mathbf{Y}=(\mathbf{G}+(2/h)\mathbf{C}+(h/2)\mathbf{K})$ since $\mathbf{G}$, $\mathbf{C}$, and $\mathbf{K}$ are all admittance. We can derive the following theorem.

Theorem 3: The admittance matrix $\mathbf{Y}$ is symmetric and positive definite.

Proof: Since $\mathcal{K}$ was shown to be SPD from the preceding discussion, $\forall z$

$$z^T\mathbf{K}z = z^T\left(\mathbf{A}_l^T\mathcal{K}\mathbf{A}_l\right)z = (\mathbf{A}_l z)^T\mathcal{K}(\mathbf{A}_l z) > 0. \quad (28)$$

Both $\mathbf{G}$ and $\mathbf{C}$ are SPD. Therefore, $\forall z$

$$z^T\mathbf{Y}z = z^T\left(\mathbf{G}+\frac{2}{h}\mathbf{C}+\frac{h}{2}\mathbf{K}\right)z$$
$$= z^T\mathbf{G}z + z^T\left(\frac{2}{h}\mathbf{C}\right)z + z^T\left(\frac{h}{2}\mathbf{K}\right)z$$
$$> 0.$$

$\mathbf{Y}$, thus, is proven to be SPD. ∎

From Theorem 3, the Cholesky decomposition or the preconditioned conjugate gradient iterative method [17] is applicable for the NA formulation. Using the reluctance extraction algorithm shown in the previous section, $\mathcal{K}$ is sparse, which makes $\mathbf{Y}$ also a sparse matrix. This result is derived from our previous works [17], [18]. Another work [16] has made similar discovery independently.

C. Implementation Considerations: A Comparison Study

Since the MNA matrix $(\tilde{\mathbf{G}}+(2/h)\tilde{\mathbf{C}})$ in (22) is asymmetric, LU factorization is unavoidable even when we switch the sign of $-\mathbf{A}_l$ and $\mathcal{L}$ in (21) to be a symmetric but indefinite matrix. On the contrary, matrix $\mathbf{Y}$ in the NA is SPD, which makes the Cholesky decomposition applicable. There are several well-known benefits of the Cholesky decomposition over the LU decomposition. First, the runtime and memory requirements of the Cholesky decomposition are half as those of the LU decomposition, since the former can take the advantage of the symmetricity. Second, the LU decomposition requires advanced reordering and pivoting algorithms to enhance numerical conditions and avoid breaking down. It has been shown that the accuracy of the Cholesky decomposition is always the best regardless of the matrix ordering. Matrix reordering for the Cholesky is usually performed only for fill-in reduction and only topologically. The sparsity of the NA formulation is often slightly worse than MNA since $\mathbf{K}=\mathbf{A}_l^T\mathcal{K}\mathbf{A}_l$ introduces more matrix entries than $\mathcal{L}$. However, we believe that the additional entries are offset by the saving of symmetricity.

It is well known that the computation time of the factorization is dominated by the number of fill-ins and the matrix ordering plays a crucial role to the fill-ins. The reduction of fill-ins not only saves the runtime of the decomposition but also
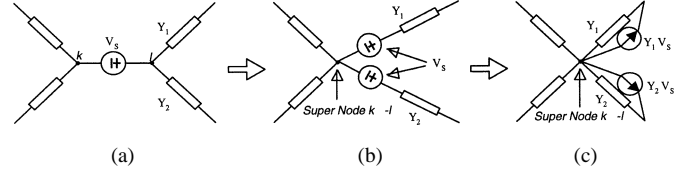

Fig. 6. Voltage source transformation. (a) The original circuit. (b) Group nodes k and l and form a super node $k-l$. Transform voltage sources to Norton equivalent currents.

has tremendous benefit for later transient simulation since we have a smaller amount of matrix entries in the triangle matrices. It is also known that it is easier and more efficient to perform matrix reordering to symmetric matrices. About matrix reordering algorithms, there are just so many of them such as reverse Cuthill-McKee (RCM), minimum degree (MD), nested dissection (ND) methods, and their variants. From the authors' knowledge and experimental results, we discover that MD is one of the most efficient ways to reduce fill-ins for time-domain circuit simulators.

D. Handle Independent Voltage Sources

In case there are independent voltage sources in the circuit, we have to add extra current variables in the MNA equations. Thus, (20) becomes

$$\begin{bmatrix}\tilde{\mathbf{G}} & \mathbf{A}_v^T \\ \mathbf{A}_v & 0\end{bmatrix}\begin{bmatrix}\mathbf{x} \\ \mathbf{i}_v\end{bmatrix} + \begin{bmatrix}\tilde{\mathbf{C}} & 0 \\ 0 & 0\end{bmatrix}\begin{bmatrix}\dot{\mathbf{x}} \\ \dot{\mathbf{i}}_v\end{bmatrix} = \begin{bmatrix}\mathbf{b} \\ \mathbf{v}_s\end{bmatrix} \quad (29)$$

where $\mathbf{A}_v$ and $\mathbf{v}_s$ are the adjacency matrix and vector of values for voltage source elements, respectively. In our implementation of the NA, we transform voltage sources into Norton equivalent circuits as shown in Fig. 6.

If the voltage source connects to the R or C elements, this method can be easily implemented. Norton equivalent circuits for R and C elements are available. However, coupling of inductances makes this transformation inapplicable for L lements. Consider the circuit shown in Fig. 7(a), which shows a voltage source connecting to one terminal of two coupled inductances. Using frequency-domain analysis, the current–voltage equations on its two ports are as follows:

$$I_1 = \frac{K_{11}}{s}(V_1-V_K) + \frac{K_{12}}{s}V_2$$
$$I_2 = \frac{K_{12}}{s}(V_1-V_K) + \frac{K_{22}}{s}V_2.$$

These two equations can be rewritten as

$$I_1 = \frac{K_{11}}{s}V_1 + \frac{K_{12}}{s}V_2 - \frac{K_{11}}{s}V_K$$
$$I_2 = \frac{K_{12}}{s}V_1 + \frac{K_{22}}{s}V_2 - \frac{K_{12}}{s}V_K$$

which can be represented as the circuit shown in Fig. 7(b). The voltage source is replaced by current sources. Since conductance (G), capacitance (C), and reluctance (K) are all admittances, they share similarities in equivalent circuit transformation. Thus, it can be applied to the NA analysis.

IV. Experimental Results

We developed our INDUCTWISE reluctance extractor and simulator in C/C++ programming language. The extractor
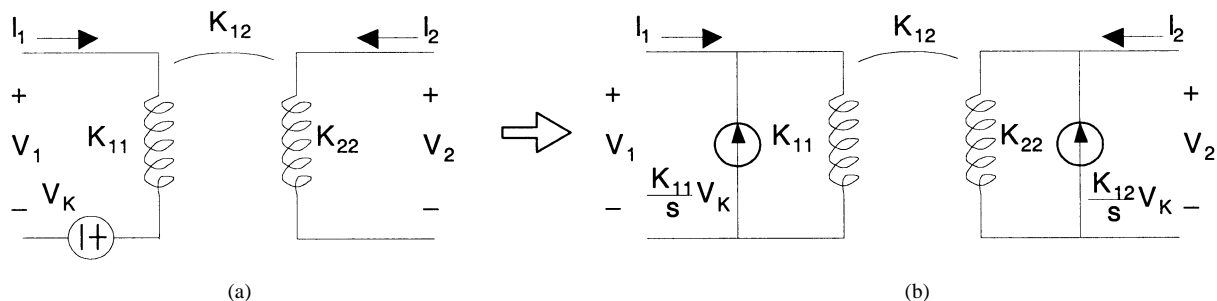
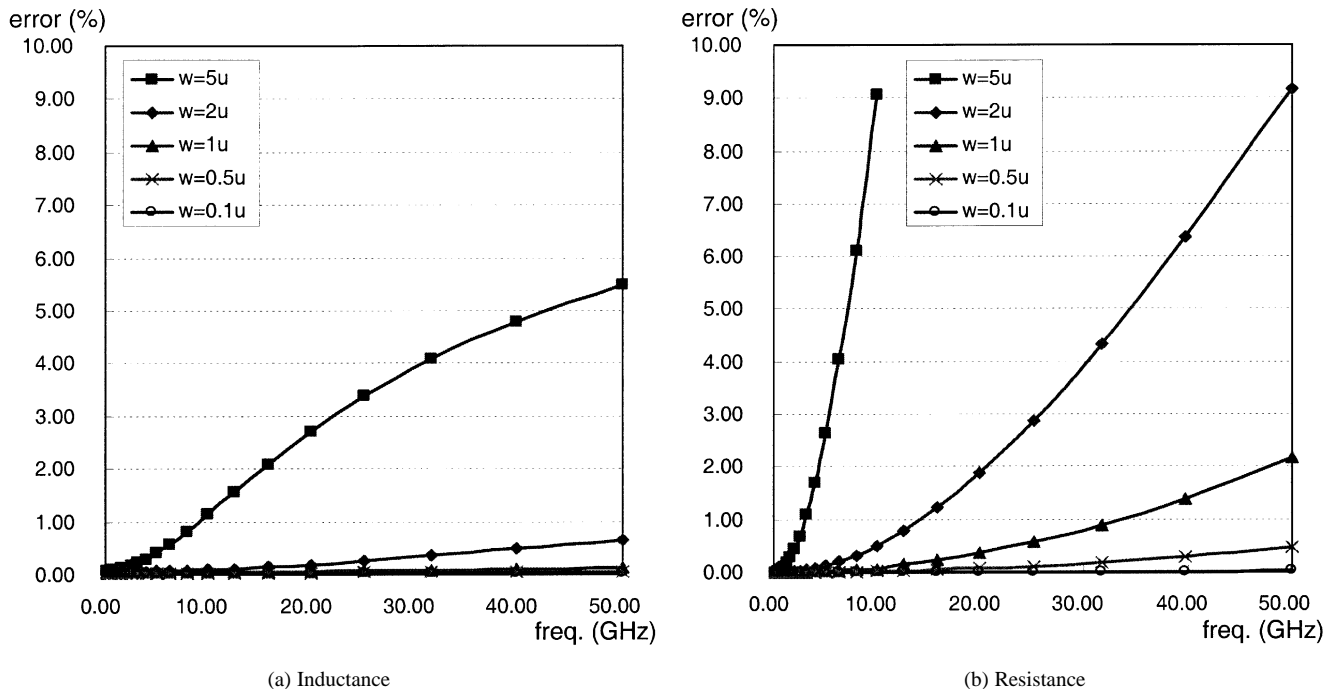Fig. 7. Norton equivalent transformation for reluctance elements.

(a) Inductance

(b) Resistance

Fig. 8. Errors of (a) inductance and (b) resistance for INDUCTWISE without adaptive discretization.

implements our WSA-based K-method. The simulator implements both MNA and NA solutions, which is able to simulate circuits with inductance and reluctance elements. Simulations are run on an Intel Pentium IV 1.4-GHz system with RedHat 7.2 Linux operating system.

A. Accuracy of Inductance Extraction

INDUCTWISE extractor utilizes formulae-based inductance calculation [19], [20] to obtain the inductance values of interest. Figs. 8 and 9 show the errors of inductance and resistance values of INDUCTWISE. We compare self inductance and resistance values extracted from INDUCTWISE with those from FastHenry [6], in which each conductor is discretized into 100 filaments. The height of the conductor is 0.28 μm and its length is 100 μm. Five different widths (0.1, 0.5, 1, 2, 5 μm) are tested over 0.1 ∼ 50 GHz operation frequencies. In Fig. 8, no discretization is performed for each conductor, and it shows that the formulae-based inductance extraction have less than 1% of error when the operation frequency is under 10 GHz and the wire width is less than 2 μm. For those wider conductors or higher frequency components, finer discretization is necessary to preserve accurate extraction. We, thus, adaptively cut each

of the conductors into 5 filaments according to the skin depth and repeat the preceding experiment, whose result is shown in Fig. 9. It's clear that both resistance and inductance values have less than 1% of error when the operation frequency is less than 50 GHz, which is highly improved.

Therefore, according to the width and maximum frequency (user defined) INDUCTWISE dynamically adjusts the number of filaments for each conductor to achieve accurate extraction with the smallest number of filaments. Unlike FastHenry, INDUCTWISE does not combine filaments to equivalent RL values, but keeps these discretized RL elements in the subsequent time-domain simulation. There are two reasons why we implement our extraction tool in this way. First, although introducing additional elements into time-domain simulation hurt the runtime of our simulator, it results in more accurate simulation. When performing on-chip circuit simulation, there are usually more than one frequency components. Using equivalent RL values would cause the time-domain simulation to be accurate only for the specified frequency component. Second, from Figs. 8 and 9, we know that only a few filaments are needed for wide conductors. In addition, parallel connected wires are preferable to wide interconnects in VLSI designs in

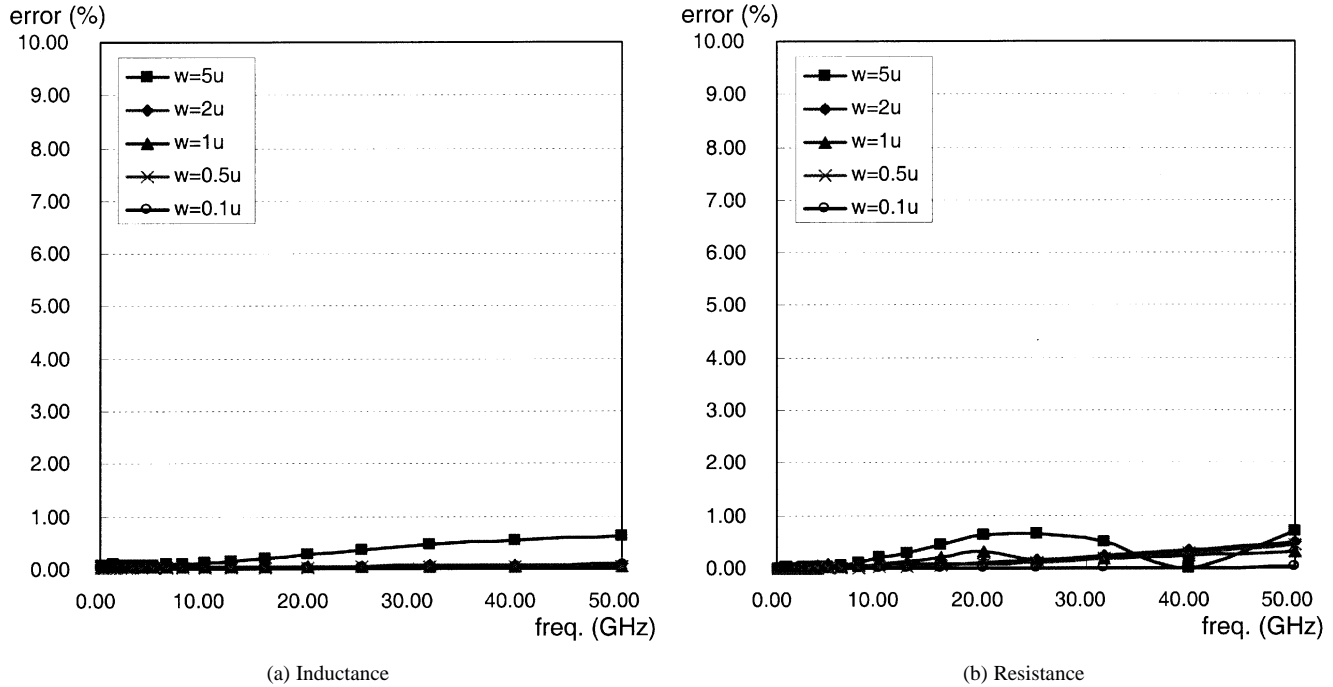(a) Inductance   (b) Resistance

Fig. 9.   Errors of (a) inductance and (b) resistance for INDUCTWISE with adaptive discretization.

TABLE III
ACCURACY OF THE WSA FOR DIFFERENT SHIELDING LEVELS AND ESFs (154 CONDUCTOR SEGMENTS)

Shielding Level	ESF	Density	Attacker		Faraway victim	
			1st peak error	2nd peak error	1st peak error	1st droop error
1	0.0	4.0%	3.21%	-2.26%	-33.52%	-51.72%
1	0.5	4.6%	0.55%	0.62%	-26.46%	-37.70%
1	1.0	5.0%	0.52%	0.82%	-27.19%	-35.63%
2	0.5	8.1%	-0.33%	0.72%	-11.59%	-22.99%
3	0.5	11.4%	0.12%	1.23%	-11.30%	-22.07%
5	0.5	17.5%	0.20%	1.91%	-3.85%	-4.85%

order to avoid skin effect. Thus, very wide conductors would be in the minority for on-chip parasitic extraction process.

B. Accuracy of Reluctance Approach

Table III shows the accuracy information of the time-domain simulation using the WSA-based reluctance extraction with a 154-conductor circuit. Each driving end has a voltage source connected to the nearest ground wire, and each loading end has load capacitors connected to both the power and ground lines. We activate one of the driving sources, which is called attacker, with a 1-volt step function, and observe the responses of the loading ends of both the attacker and a faraway victim that is ten conductors away from the attacker. From Table III, we find that the shielding level and the ESF affect the accuracy in the following manner. Enlarging the ESF improves the accuracy on the attacker, but not the victim. On the contrary, enlarging the shielding level helps improve the accuracy on the faraway victim, but has less effectiveness on the attacker. Fig. 10(a) and (b) shows the waveforms for different parameters and illustrates this trend. In this case, shielding level 1 with 0.5 ESF already approaches the exact solution very well for the active conductor, and a higher shielding level even improves the faraway accuracy more. The WSA with shielding level 5 and ESF 0.5 almost

matches the exact solution. From this result, by choosing a sufficient shielding level and ESF, we can capture the inductance effect precisely with very few mutual reluctance elements.

C. Runtime Comparison

Table IV shows the runtime information of INDUCTWISE. The drive and load RC setup is the same as described in the previous paragraph. In order to have fair comparison with FastHenry, we set only one filament per conductor for both INDUCTWISE and FastHenry. It shows that INDUCTWISE is about $8\times$ faster than FastHenry under the same accuracy level. By using our sparse reluctance solution, the extractor can improve another $26.2\times$.

For time-domain simulation, we perform 200 timesteps for each simulation. For the 1000-conductor case, SPICE3 [21] takes 23322.3 s to solve the exact solution while INDUCTWISE only takes 43.7 s ($534.3\times$ speedup). Due to the superlinear dependence of solution time on matrix size, the speedup will be more dramatic for larger systems. By setting the shielding level to 3 and the ESF to 0.5, the sparse reluctance method improves an extra $488\times$. INDUCTWISE can extract and simulate a 100K-conductor RKC circuit within 13.5 min. The runtime of the sparse reluctance approach is almost linear.
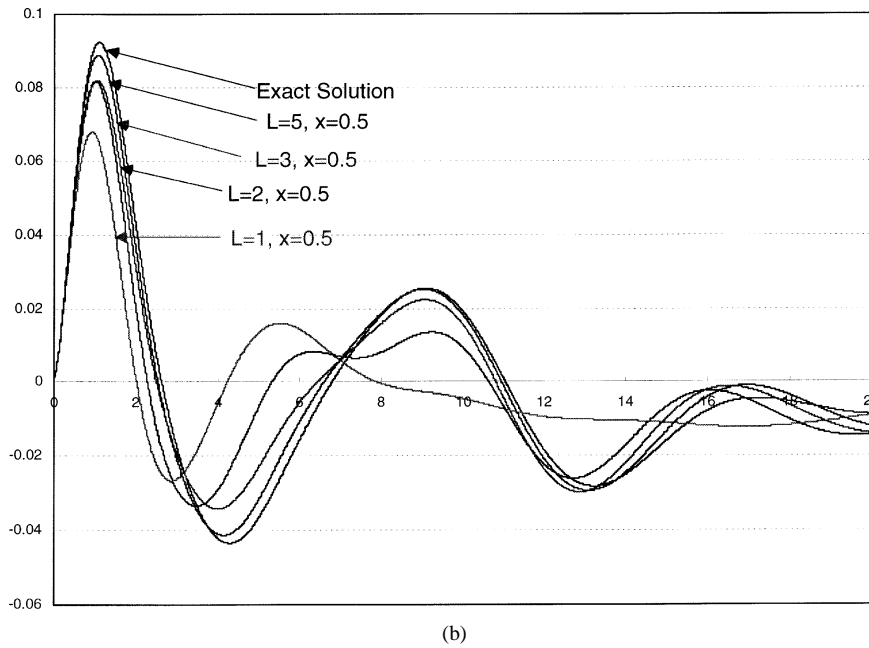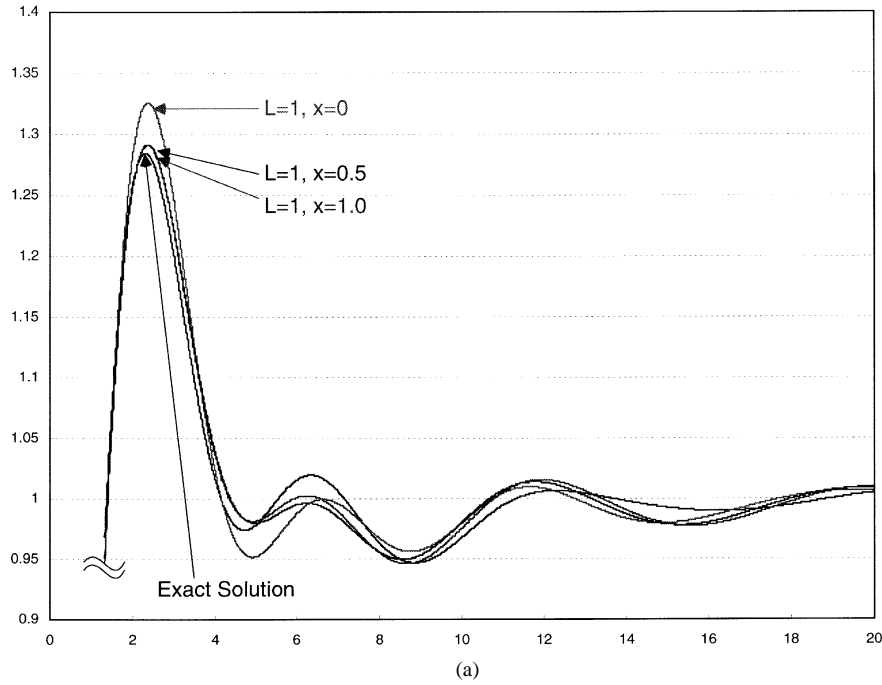
Fig. 10.   Waveforms of (a) Attacker at different ESFs and (b) Faraway victim at different shielding levels.

TABLE IV
RUNTIME COMPARISON BETWEEN INDUCTWISE (RLC AND RKC), FASTHENRY, AND SPICE3 (RLC)

# of conductors	Extraction			Simulation		
	FastHenry	INDUCTWISE		SPICE3	INDUCTWISE	
	Full $\mathcal{L}$	Full $\mathcal{L}$	Sparse $\mathcal{K}$	Full $\mathcal{L}$	Full $\mathcal{L}$	Sparse $\mathcal{K}$
154	3.8s	1.6s (2.4x)	0.6s (2.7x)	22.7s	0.4s (56.8x)	0.2s (2.0x)
500	126.3s	17.3s (7.3x)	2.6s (6.7x)	1794.3s	7.1s (252.7x)	0.7s (6.4x)
1,000	595.5s	69.1s (8.6x)	5.3s (13.1x)	23322.3s	43.7s (534.3x)	1.5s (29.9x)
2,000	2029.8s	275.2s (7.4x)	10.5s (26.2x)	>4days	561.6s	3.2s (488x)
4,000	-	-	21.2s	-	-	6.5s
8,000	-	-	42.6s	-	-	14.6s
10,000	-	-	53.4s	-	-	18.6s
100,000	-	-	534.0s	-	-	270.4s

V. CONCLUSION

A comprehensive solution for calculating the on-chip inductance effect was proposed in this paper. We developed a robust, efficient, and accurate inductance extraction and simulation tool, INDUCTWISE, extending the state-of-the-art inductance extraction technique, the K-method. We introduced the concept of reluctance, pointed out the stability issue in the K-method, and retrieved this method with theoretical explanation and an auxiliary algorithm (RBA). The WSA further allows the reluctance extraction for general geometry configurations. With the NA formulation, INDUCTWISE can directly take reluctance elements into simulation. By using the reluctance technique, both extraction and simulation have almost linear complexity.

ACKNOWLEDGMENT

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