ESPRIT: A Compact Reluctance Based Interconnect Model Considering Lossy Substrate Eddy Current

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Abstract— **With the advancement of radio frequency mixed-signal ICs, lossy silicon substrate has significant impact on the already complicated interconnect modeling issue. To account for the substrate loss, the traditional electromagnetic methods are often computationally prohibitive for large scale VLSI geometries. In this paper, we extend the traditional PEEC model to consider the substrate eddy current loss based on the complex image theory and the skin and proximity effects by discretization of conductors. To deal with even larger scale of interconnects, we present a reluctance based model, ESPRIT, to enhance the extended PEEC model to use reluctance by equipping it with an advanced windowing algorithm to further reduce the model size and runtime. Detail comparisons with state-of-the-art tools such as FastHenry and Momentum demonstrate that ESPRIT is within 1% accuracy while providing over 100X speedup.**

I. Introduction

Due to the proliferation of mixed analog-digital system and radio frequency integrated circuit (RFIC), the development of efficient interconnect models for such a system is made difficult because of the lossy nature of the silicon substrate. In particular, the creation of eddy currents in the conductive silicon substrate can lead to significant interconnect inductance loss. An interconnect system analysis without considering the lossy substrate effect will result in an over-designed network and waste chip resources.

With the increasing clock frequency and integration density, intentional and unintentional inductance effects gradually rise. One major problem of inductance analysis is the unknown current return path. Fortunately, the PEEC (Partial Equivalent Element Circuit) method has been widely adopted to deal with this issue [1]. However, since PEEC model assumes current return paths at infinity, extremely dense partial inductance matrices are usually generated which dramatically increases both model size and simulation runtime.

For this reason, various inductance sparsification techniques have been introduced to alleviate this problem [2]–[4]. In particular, the reluctance-based method [5] [6] has been proposed by Hao Ji et al. Since reluctance has higher degree of locality similar to capacitance, only a small number of neighbors need to be considered, and hence reluctance matrix for circuit simulation is very sparse compared to partial inductance matrix.

Moreover, the traditional PEEC approach does not take the substrate loss effect into consideration and hence cannot capture the inductance loss due to the formation of eddy currents in the conductive substrate. Although several works have been proposed to resolve this issue by constructing three dimensional linear substrate models [7]–[9], most of these approaches employ a numerical finite difference based method by spatially discretizing a large volume of silicon bulk under the conductor system and hence will lead to equivalent circuits prohibitive in size.

In this paper, we propose an accurate and efficient method to extend the PEEC model to consider the substrate eddy current loss based on the complex image theory [10], which has been recently used in RFIC regime to accurately capture line impedances of microstrips [11] [12] and spiral inductors [13] on lossy silicon substrates. The complex image theory generates the complex images of interconnects based on the configuration of substrate structure instead of discretizing the substrate and hence can result in very compact models for interconnects.

To deal with millions of interconnects and their images, we enhance the extended PEEC model to use reluctance element with an extended window searching reluctance extraction algorithm. Finally, since this new model, ESPRIT, includes mutual resistances and reluctances, in order to be applicable to general circuit simulators, SPICE compatible models for mutual resistance and reluctance are also provided. Detail comparisons with state-of-the-art tools such as FastHenry and Momentum demonstrate that ESPRIT is within 1% accuracy while providing over 100X speedup.

II. Complex Image Theory

For frequencies up to a few Giga Hertz, the wavelength of the magnetic fields far exceeds a typical die's dimension. Thus we can make magneto-quasi-static approximations.

Under this assumption, for a z-direction current, only the z-component of the magnetic potential $\mathbf{A}$ is nonzero, thus the substrate diffusion equation can be reduced to a two dimensional EM problem:

$$\bigtriangledown^2 \mathbf{A}_z(x,y) - \mu\sigma \frac{\partial}{\partial t}\mathbf{A}_z(x,y) \quad = \quad 0 \qquad (1)$$

By constructing the Green's function, the solution can be

expressed as:

$$\mathbf{A}_z(x,y)=\int G(x,y|x',y')\mathbf{J}_z(x',y')dx'dy' \qquad (2)$$

where $\mathbf{J}_z(x,y)$ is the current distribution of a line current located above the substrate.

Without loss of generality, we assume that a unit line current is located at $(x'=0,y')$, with the consideration of the finite thickness of the substrate and the presence of a ground plane, the Green's function $G(x,y|x'=0,y')$ can be expressed as [11]:

$$G(x,y|x'=0,y')=$$
$$\frac{\mu_0}{2\pi}\int_0^{\infty}[\frac{e^{-k|y-y'|}}{k}-\frac{p-k}{p+k}e^{kd}\frac{e^{-k(y+y'+d)}}{k}]cos(kx)dk \qquad (3)$$

where

$$\gamma = \sqrt{j\omega\mu_0\sigma_{si}} \qquad (4)$$
$$q(k) = \sqrt{k^2+\gamma^2} \qquad (5)$$
$$p(k) = q(k)coth[q(k)h_{si}] \qquad (6)$$

μ_0 is the permeability of free space, σ_{si} is the bulk conductivity, h_{si} is the thickness of the substrate, while $coth[x]$ is the hyperbolic cotangent function.

The kernel of the integral in Eq. 3 has two terms. The first term can be attributed to the physical line current located at $(x'=0,y')$, while the second term is due to an image line current located at $y=-(y'+d)$. This approximation holds when the coefficient of the second term, $\frac{p-k}{p+k}e^{kd}$, is approximated by constant one. By applying the Taylor expansion of $\frac{p-k}{p+k}e^{kd}$ at $k=0$ and neglecting high order terms, we obtain that this requirement can be satisfied when

$$d = (1-j)\cdot\delta_{si}\cdot tanh[\frac{(1+j)h_{si}}{\delta_{si}}] \qquad (7)$$

where $\delta_{si}=1/\sqrt{\pi f\mu_0\sigma_{si}}$ is the skin depth of the bulk silicon and $tanh[x]$ is the hyperbolic tangent function.

Thus the eddy current effect in the lossy substrate and the ground plane can be approximated by an image current located at the complex distance d below the substrate surface. Alternatively, an image ground plane can be placed at $d/2$ below the surface to represent the currents both in the substrate and the ground plane.

III. EXTENDED PEEC MODEL

For interconnects within metal layer i, which has a distance d_{Mi} above the substrate, according to the complex image theory, the lossy silicon substrate effect can be approximated by placing a complex image plane below metal layer i at an effective complex distance, h^i_{eff}. If we denote the thickness of oxide and silicon bulk as h_{ox} and h_{si} respectively, by using Eq. 7, the effective complex distance of metal layer i is given by:

$$h^i_{eff}=d_{Mi}+h_{ox}+\frac{1-j}{2}\cdot\delta_{si}\cdot tanh[\frac{(1+j)h_{si}}{\delta_{si}}] \qquad (8)$$

Since for every metal layer of the on-chip conductor system, only the first term d_{Mi} in Eq. 8 is different, a common complex image plane is shared by all metal layers. Based on the method of image, the common complex image plane can be substituted by image conductors which are at a distance $2h^i_{eff}$ below the physical conductors in metal layer i.

Besides the lossy substrate effect, as the frequency goes high, the current in a physical conductor is no longer evenly distributed, which leads to significant changes in resistance and inductance values. In order to obtain wide band accuracy, those effects, namely skin effect and proximity effect, also need to be modeled. For capturing both skin and proximity effects, conductors have to be discretized into filaments so as to account for the non-uniform distribution of current within conductors [14].

The extended PEEC model, which is shown in Fig. 1, is obtained by the application of complex image theory and the discretization of both the physical and image conductors into filaments.

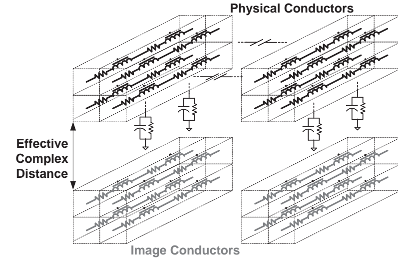

Fig. 1. Extended PEEC model

The complex inductance matrix for the conductor system with n filaments is given by:

$$L(h_{eff})=L_{freespace}-L_{image} \qquad (9)$$

$L_{freespace}$ is the inductance matrix without considering the lossy substrate, i.e. in free space. L_{image} is the mutual inductance matrix between physical and image filaments. The calculation of L_{image} depends on the effective complex distance h_{eff}, thus $L(h_{eff})$ will be frequency and process parameters dependent.

Since $L(h_{eff})=L(\omega)+R(\omega)/j\omega$, the complex inductance matrix can be interpreted as follows:

$$L(\omega)=Real[L(h_{eff})] \qquad (10)$$

and

$$R(\omega)=-\omega Imag[L(h_{eff})]+R_{DC} \qquad (11)$$

where $L(\omega)$ and $R(\omega)$ are the frequency dependent partial inductance and resistance matrix respectively. R_{DC} is a diagonal matrix including DC resistances of the physical filaments. It can be seen that $R(\omega)$ contains off diagonal terms which represent mutual resistances. We will address the mutual resistance modeling problem in the following section.

IV. SPICE COMPATIBLE RELUCTANCE-BASED MODEL

In the previous section, we present how to obtain partial inductance matrix $L(\omega)$ and resistance matrix $R(\omega)$ by

using complex image theory. However, $L(\omega)$ and $R(\omega)$ are extremely dense due to the globe effect of partial inductance coupling. Therefore, a more practical modeling approach is necessary to obtain circuit model of manageable size.

A. Physical Meaning of Partial Reluctance

Reluctance based methods have been extensively used recently because reluctance has better locality than inductance. The partial reluctance matrix K is defined as the inverse of the partial inductance matrix L.

$$K = L^{-1} \tag{12}$$

Since $LI = \Phi$ and by applying the Stoke's theorem:

$$\Phi = \int Bds = \int \bigtriangledown \times Ads = \int Adl \tag{13}$$

the partial inductance matrix for a system including n conductors will be:

$$\begin{bmatrix} L_{11} & L_{12} & \cdots \\ L_{21} & L_{22} & \cdots \\ L_{n1} & L_{n2} & L_{nn} \end{bmatrix} \begin{bmatrix} I_1 \\ \vdots \\ I_n \end{bmatrix} = \begin{bmatrix} \int A_1 dl_1 \\ \vdots \\ \int A_n dl_n \end{bmatrix} \tag{14}$$

where A_i is the vector potential in conductor i. Hence the partial reluctance matrix can be obtained as follows:

$$\begin{bmatrix} K_{11} & K_{12} & \cdots \\ K_{21} & K_{22} & \cdots \\ K_{n1} & K_{n2} & K_{nn} \end{bmatrix} \begin{bmatrix} \int A_1 dl_1 \\ \vdots \\ \int A_n dl_n \end{bmatrix} = \begin{bmatrix} I_1 \\ \vdots \\ I_n \end{bmatrix} \tag{15}$$

The globe coupling effect of partial inductance is caused by the artificial assumption that the current return path is at infinite. During partial inductance extraction, we apply a unit current source on the aggressor conductor at infinity and force the currents in victim conductors to be zero by applying zero current sources at infinity. Since in this scenario the only magnetic field is generated by the current in the aggressor and no other magnetic fields cancel its effect, it can propagate far away and give rise to a dense partial inductance matrix.

However, when calculating the self and mutual reluctances for conductor j, we need to set a unit magnetic flux for the jth conductor, and zero flux for all others. In order to satisfy this configuration, we need to apply an unit vector potential on the aggressor and at the same time pose negative vector potentials on victims to cancel the magnetic field generated by the aggressor. Therefore, the currents flowing in aggressor and victims are basically of opposite direction and the magnetic field of the aggressor is mostly cancelled by victim magnetic fields and cannot propagate faraway. This explains why partial reluctance has better locality than partial inductance.

B. Extended Window Selection Algorithm

In stead of directly calculating partial inductance matrix and inverting it to obtain partial reluctance matrix, most existing reluctance extraction tools are based on window selection algorithms, such as [15]. Here we propose an extended window selection algorithm to consider both physical conductors and their images.

- *Effective Search Window (ESW)*: Extend the physical aggressor along its length by a *window extension factor (WEF)* and obtain the *effective window width (EWW)*. Then, the ESW is defined by sweeping in the direction perpendicular to the length of the aggressor to infinity with the EWW.
- *Conductor Shielding Level (CSL)*: The CSL of the aggressor is defined as 0, which is the highest level. Conductors outside ESW are of CSL ∞, the lowest level. A conductor i is directly shielded by conductor j if conductor j can be reached by some points along the length of conductor i within ESW without encountering any other conductors. A conductor is of CSL k+1, if the minimum CSL of conductors directly shielding it is k.
- *Conductor Group of CSL k*: Conductor group of CSL k contains two parts. The physical part includes the physical aggressor and its victim conductors of CSL no larger than k. The image part includes images of physical conductors in the physical part. The union of these two parts gives conductor group of CSL k.

We illustrate our extended window selection algorithm through a small example shown in Figure 2. If the current aggressor is conductor 1, its CSL is 0. Conductor 3 and 4 are of CSL 1; Conductor 5, 6, 7 and 8 are of CSL 2 while conductor 9 is of CSL 3. Conductor 2 is outside the ESW and hence its CSL is ∞. Conductor group of CSL 1 includes physical conductors 1, 3, 4 and image conductors $1'$, $3'$ and $4'$.

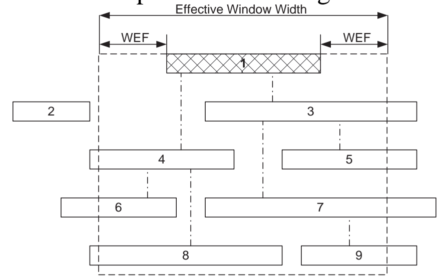

Fig. 2. Extended Window Selection Algorithm

Our frequency dependent reluctance-based interconnect model, ESPRIT, is based on the combination of the extended PEEC and the above window selection algorithm. For each conductor, we search its conductor group of CSL k and calculate the small $L(\omega)$ and $R(\omega)$ for this conductor group after proper discretization according to conductor skin depth. Then the small $L(\omega)$ for this conductor group is inverted to obtain the small $K(\omega)$ matrix. The final circuit model is assembled by using those small $K(\omega)$ and $R(\omega)$ matrices.

Since ESPRIT includes mutual resistances and reluctances, in order to avoid significant modifications on general simulation tools, we need to consider their SPICE compatible models, which can be obtained from their branch equations respectively. The branch equation of self and mutual resistances is given by

$$V_i = \sum_{j=1}^{n} R_{ij} I_j = R_{ii} I_i + \sum_{j=1, j\neq i}^{n} R_{ij} I_j \tag{16}$$

where R_{ii} is self resistance and R_{ij} is the mutual resistance between R_{ii} and R_{jj}. Eq. 16 can be rewritten as

$$V_i = R_{ii} I_i + \sum_{j=1, j \neq i}^{n} \frac{R_{ij}}{R_{jj}} (R_{jj} I_j) \quad (17)$$

If we view $R_{ii} I_i$ as the voltage drop across the self resistance R_{ii}, V_i is then equal to the sum of the voltage drop on a self resistance R_{ii} and serially connected voltage control voltage sources (VCVS). These VCVSs are controlled by voltages on other self resistances which originally have mutual resistances with R_{ii}. Therefore, Eq. 17 can be used to construct SPICE compatible model for mutual resistances, which is shown in Figure 3.(a), where $V^R_{VCVS} = \sum_{j=1, j\neq i}^{n} \frac{R_{ij}}{R_{jj}} V_{jj}$.

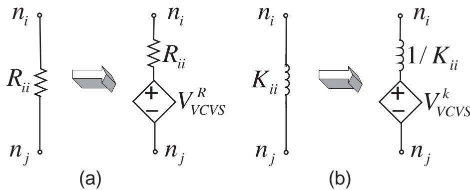

Fig. 3. SPICE Compatible Model for (a) mutual resistance (b) reluctance

SPICE compatible model for reluctance can be derived by similar method. It includes a self inductance $1/K_{ii}$ and serial VCVSs $V^K_{VCVS} = -\sum_{j=1, j\neq i}^{n} \frac{K_{ij}}{K_{jj}} V_{jj}$ shown in Figure 3.(b). By applying those equivalent circuit models, ESPRIT can be fully accepted by general simulators.

V. Experimental Results

Extensive experimental results are reported to show the efficiency and accuracy of our new interconnect model ESPRIT.

To validate the new modeling approaches and to illustrate the accuracy, we first compare the inductance values computed by the enhanced PEEC model with FastHenry [14] and a more rigorous full wave EM analysis tool, HP-Momentum. Under

TABLE I
INDUCTANCE VALUE COMPARISION

Frequency (gHz)	HP Momentum	FastHenry			EPEEC		
		Value (pH)	Error (%)	Time (s)	Value (pH)	Error (%)	Time (s)
5	81.1102	87.5368	7.923	558.1	81.1167	0.008	<1
10	76.8060	85.8109	11.72	569.2	76.4245	0.496	<1
15	74.0398	84.7232	14.42	588.3	73.5964	0.599	<1

20GHz, the enhanced PEEC gives inductance values that are extremely close to full wave simulation results (within 1% error) and shows over 100X speedup compared to FastHenry.

The following experiment is run to show the computational complexity of ESPRIT. The testing conductor system includes 2000 conductor segments which are in a power/ground network from metal layer 7 to 5. Without considering the substrate, PEEC takes about 25.316s to assemble the model, while the enhanced PEEC spends about 59.131s to model the lossy substrate effect. However, they both contain 282,125 elements. While applying ESPRIT by searching neighboring of shielding level two, it takes only 5.368s to obtain the circuit model with 3,632 elements.

The waveforms of the enhanced PEEC at different frequencies are shown in Fig. 4.(a). Also the responses in Fig. 4.(b) demonstrate that ESPRIT has much smaller model size while maintaining less than 3% error compared to the enhanced PEEC model.

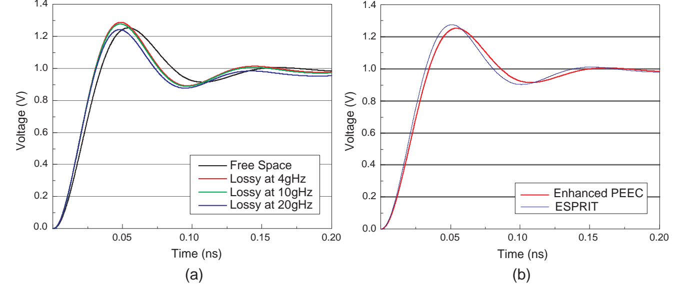

Fig. 4. The Enhanced PEEC vs. ESPRIT

VI. Conclusion

A new reluctance-based interconnect model ESPRIT considering the loss substrate effect is presented in this paper. It's obtained by combining an enhanced PEEC model with an extended window-based reluctance extraction algorithm. Extensive simulation results demonstrate that ESPRIT has extremely high accuracy and significantly small model size.

References

[1] A. E. Ruehli, "Inductance calculatioin in a complex integrated circuit environment," *IBM Journal of Research and Development*, Sep 1972.
[2] B. Krauter and L. T. Pileggi, "Generating sparse partial inductance matrices with guaranteed stability," *ICCAD*, Nov 1995.
[3] K. L. Shepard and Z.Tian, "Return-limited inductances: A practical approach to on-chip inductance extraction," *Computer Aided Design of Integrated Ciurcuits and Systems*, Apr 2000.
[4] K. Gala, V. Zolotov, R. Panda, B. Young, J. Wang, and D. Blaauw, "On-chip inductance modeling and analysis," *DAC*, Jun 2000.
[5] A. Devgan, H. Ji, and W. Dai, "How to efficiently capture on-chip inductance effects:introducing a new circuit element k," *ICCAD*, 2000.
[6] H. Ji, A. Devgan, and W. Dai, "Ksim: A stable and efficient rkc simulator for capturing on-chip inductance effect," *ASPDAC*, Jun 2001.
[7] R. Gharpurey and R. G. Meyer, "Modeling and analysis of substrate coupling in integrated circuits," *Custom Integrated Circuits Conference*, May 1995.
[8] B. R. Stanisic, N. K. Verghese, R. A. Rutenbar, L. R. Carley, and D. J. Allstot, "Address sunstrate coupling in mixed-mode ic's simulation and power distribution synthesis." *Solid-State Circuits*, 1994.
[9] T.-H. Chen, C. Luk, H. Kim, and C. C.-P. Chen, "Supreme: Substrate and power-delivery reluctance-enhanced macromodel evaluation," *ICCAD*, 2003.
[10] P. R. Bannister, "Applications of complex image theory," *Radio Science*, Aug 1986.
[11] A. Weisshaar and H. Lan, "Accurate closed-form expressions for the frequency-dependent line papameters of on-chip interconnects on lossy silicon substrate," *IEEE MTT-S International Microwave Symposium Digest*, May 2001.
[12] A. Weisshaar, H. Lan, and A. Luoh, "Accurate closed-form expressions for the frequency-dependent line papameters of coupled on-chip interconnects on lossy silicon substrate," *IEEE Trans. Adv. Packaging*, 2002.
[13] D. Melendy and A. Weusshaar, "A new scalable model for spiral inductors on lossy silicon substrate," *Microwave Symposium Digest*, 2003.
[14] M. Kamon, M. J. Tsuk, and J. K. White, "Fasthenry: A multipole-accelerated 3-d inductance extraction program," *DAC*, Jun 1993.
[15] G. Zhong, C.-K. Koh, V. Balakrishnan, and K. Roy, "An adaptive window-based susceptance extraction and its efficient implementation," *DAC*, Jun 2003.