1-V 7-mW Dual-Band Fast-Locked Frequency Synthesizer

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ABSTRACT

This paper presents a fully integrated 1-V, dual band, fast-locked frequency synthesizer for IEEE 802.11 a/b/g WLAN applications. It can synthesize frequencies in the range of 2.4 - 2.7 GHz with a step of 9.375 MHz, and in the range of 5.14 - 5.70 GHz with a step of 20 MHz. Simulation using 0.18-μm rf and mixed-signal CMOS technology demonstrates a total power consumption of 7-mW. An adaptive bandwidth controller is employed to achieve a fast locking time. The frequency divider combines the conventional and the extended true-single-phase-clock logics. To ensure a proper dividing function, a cascode voltage switch (CVS) topology is used in the preamplifier stage. The reference spurs at an offset of 10-MHz are as low as -80 dBc, and the phase noise at an offset of 1 MHz is lower than -118 dBc for the entire tuning range.

Categories and Subject Descriptors

B.7.m [**INTEGRATED CIRCUITS**]: Miscellaneous-*Radio Frequency Integrated Circuits*

General Terms

Design, Performance

Keywords

Frequency synthesizer, HiperLAN, Low-power design, Phase-locked loops (PLLs), Phase noise, Voltage-Controlled Oscillator (VCO), WLAN.

1. INTRODUCTION

Wireless LAN systems in the multigigahertz band, such as HiperLAN II and IEEE 802.11a/b/g, are recognized as the leading standards for high-rate data transmissions. Being intended for mobile operations, the radio transceiver has a limited power budget. The frequency synthesizer, usually implemented by a phase-locked loop (PLL), is one of the most critical blocks in terms of average current dissipation since it operates extensively for both receiving and transmitting end. The best published integrated synthesizers around 5 GHz, suitable for wireless LAN receivers, consume up to 25mW in both CMOS and bipolar realizations [1]-[3]. This high power consumption is mainly due to the power supply and the first stage of the frequency divider that often dissipates half of the total power. Due to the high input frequency, the first stage of the divider cannot be implemented in conventional static CMOS logic [4]. Instead, it is commonly realized in source-coupled logic (SCL) [5], which allows higher operating frequency, but burns more power. An efficient alternative to the first SCL divider would be an injection locking-divider described in [3]. However, this resonant divider requires a tank whose area is larger than the oscillator's tank itself, and it also suffers from pulling mechanism. Dynamic latches are known to be faster and more compact than the static ones. The extended true-single-phase-clock (ETSPC) design allows driving the dynamic latch with a single clock phase, thus avoiding the skew problem [6].

In this paper, we describe a dual band frequency synthesizer for the IEEE 802.11a/b/g WLAN applications.

The organization of paper is as follows. Section 2 describes our architecture of the frequency synthesizer which can synthesize frequencies in two bands. In Section 3 PLL building blocks are described. Section 3.1 is dedicated to the design of the VCO and describes the use of an on-chip filter to reduce the phase noise. Section 3.2 discusses about the high frequency divider and pre-amplifier stages. In section 3.3 a low voltage charge pump and an adaptive bandwidth controller that can achieve fast locking, are described. Section 4 presents the simulation results. It also includes the measurement results of our NMOS-only VCO that has separately been fabricated to test its performance, before employing it into the synthesizer.

2. SYNTHESIZER ARCHITECTURE

The frequency synthesizer block diagram is shown in Fig. 1. The output frequency is given by

$$f_o = f + Sf_{ch}. \quad (1)$$

where f is the frequency of the first channel (S=0), and f_{ch} is the channel spacing. With mode select two reference frequency can be chosen. When PLL is locked to f_{REF1} the output frequency (f_o)ranges from 5.18 - 5.8725 GHz. It can be tuned to 32 channels with a channel spacing of 20.23 MHz. On the other hand, when Mode Select block selects

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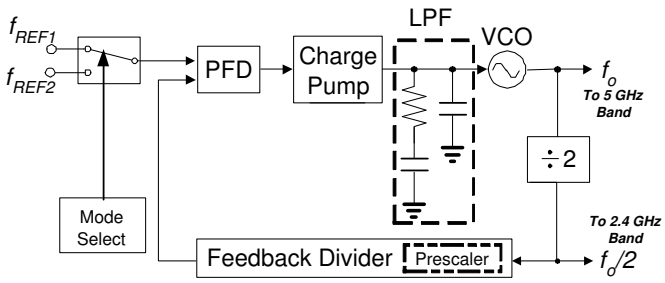

Figure 1: PLL-Based Frequency Synthesizer

f_{REF2} output frequencies in the range of 2.4- 2.7 GHz gets synthesized. It could also be tuned to 32 channels with a channel spacing of 9.375MHz. As shown in Fig.1., for 5 GHz band output frequency is simply f_o, but for 2.4 GHz band output is taken after ÷2 block, that is $f_o/2$. Fig.2. shows the channel selection block diagram. The input frequency is divided by 4 or 5 by the dual modulus prescalar and then it is fed to programmable counter wherupon a channel selection could be made.

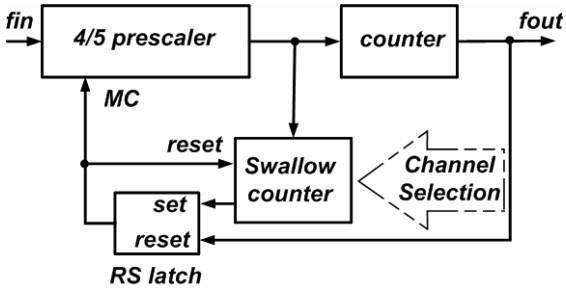

Figure 2: Channel Selection Divider

3. SYNTHESIZER BUILDING BLOCKS

3.1 Voltage-controlled Oscillator

Ring and LC oscillators are two widely used VCO types. Ring VCOs can generate quadrature signals more readily but have inferior noise performance, while LC VCOs offer better phase noise for a given power dissipation. Therefore an LC VCO topology have been used in our design. Moreover,since a large headroom with a reduced power supply voltage is required an NMOS only cross-coupled architecture has been preferred over a CMOS cross-coupled architecture[9]. The designed VCO is shown above in Fig. 3. In general, the cross-coupled differential pair is used to synthesize the negative resistance across the tank. Here, we take an advantage of the impedance appearing at the source terminal of common-gate device. We propose an 1-volt VCO that uses L to be the load of the differential pair and the L_c to be the oscillation component for a lower inductor value. The inductor between the tail transistor M4 and the NMOS switches serves two purposes. First,with the inherited parasitic capacitance of tail transistor M4, it acts as an on-chip filter and removes the high frequency noise of the M4. Secondly, it converts the common source terminal of [M1,M2] to a high impedance node for high frequency. This

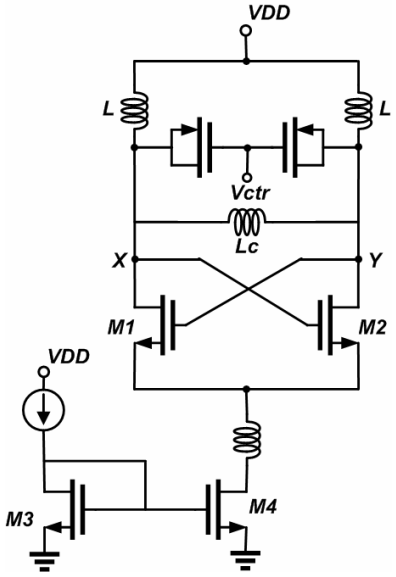

Figure 3: Our nMOS-only VCO

reduces the high frquency noise flowing from [M1,M2] to the tank. PMOS devices are used as a varactor for wide tuning range. The length of a PMOS device could be increased as to achieve the desired tuning range. The simulated power consumption including the bias circuitry is about 3.23mW.

3.2 Divider and Preamplifier

The operating frequency and power consumption are the most important parameters in high-speed digital circuits. To reduce the power consumption as compared to the static resistive load, a dynamic load that makes a changeable load, has been used. The MCML(MOS current mode logic) inverter has a restricted output swing and voltage level, since its output is periodically pulled down from the supply voltage. Therefore, we employ a MCML divider, Fig. 4, [5] to be the first divider. To achieve the desired swing and DC voltage, a source follower is commonly used as a buffer to the output stage of the divide-by-2 unit. But we propose a cascode voltage switch (CVS) to be the preamplifier, Fig.5., here. Although this preamplifier introduces an additional component in the design and thus consumes some power, it has a merit that it can distinguish an output voltage swing to Vdd and ground. This increased voltage swing can then drive the followed dynamic prescaler, Fig.5.

The prescaler embodies a synchronous divider and an asynchronous divider, Fig. 6. The prescaler has been realized using the extended true-single-phase-clock (E-TSPC) logic proposed in [6]. Compared to the classical TSPC logic, the E-TSPC avoids the stacked MOS structure that slows down the switching speed, and all the transistors are free from the body effect. For these reasons, E-TSPC logic allows higher operating frequencies and lower power supply. Although it features static power dissipation, this causes only a small increase in power dissipation, since at the frequencies of interest the dynamic power consumption is dominant over the standby current. Also, this logic allows embedding complicate logic functions within the latches. This results in very compact circuits and in a reduced number of transistors. This concept is applied in the design of the prescaler, where

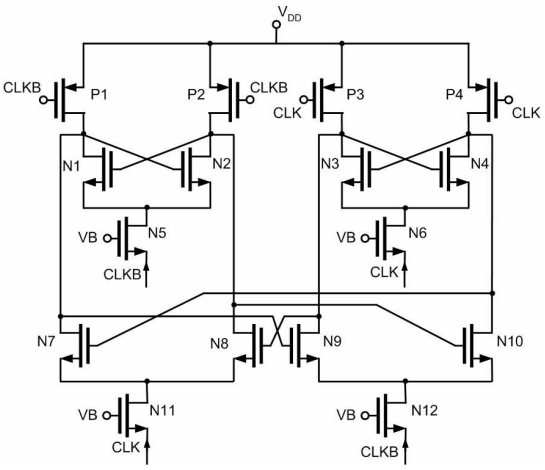

Figure 4: MCML Divider

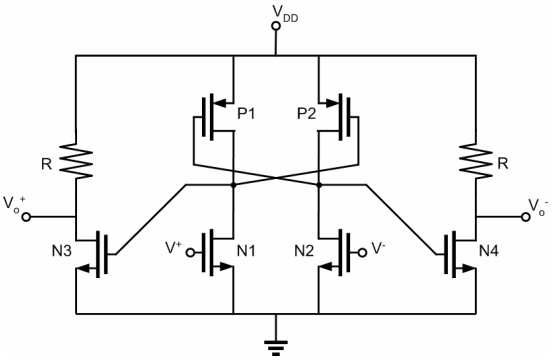

Figure 5: CVS Preamplifier

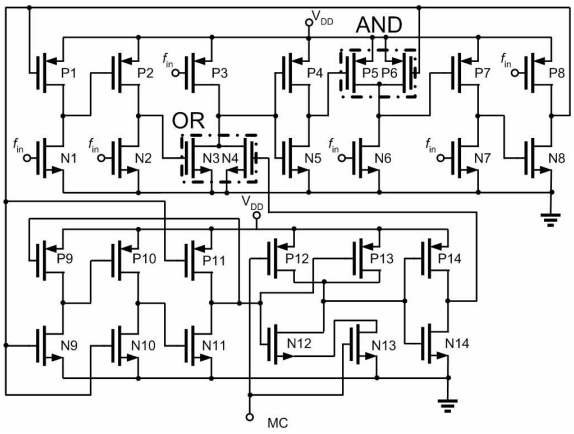

Figure 6: Dynamic Prescaler

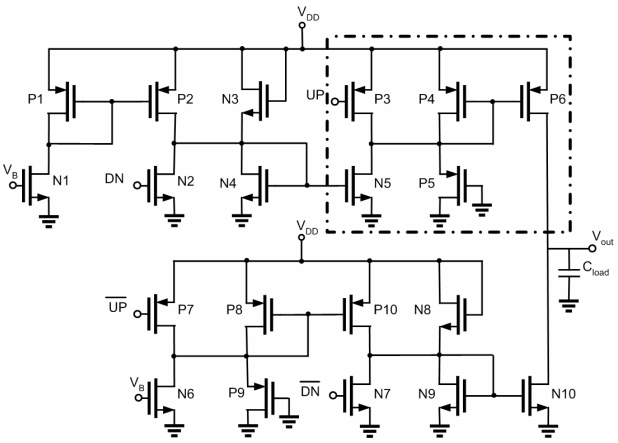

Figure 7: 1-volt Charge Pump

the AND and the OR gates are realized by adding only one transistor each. Finally, the whole prescaler dissipates 1.060 mA. And the other block shown in Fig. 2 are all build using static logic to save power consumption.

3.3 Charge Pump and Adaptive Band-width controller

To implement a very low voltage charge pump, we include a low-voltage switched push-current source, shown as a dashed box in Fig. 7, to the existing charge pump described by [8]. We propose an inter-locked structure to eliminate glitches. Compared to a conventional charge pump, it provides a more stable control voltage to the VCO. Here it should be noted that any jump in V_{out} adds an undesirable spurious tones and phase noise to the output signal of the VCO. To understand the implementation, this circuit can be partitioned into two stages. One is formed by MOS P3, P4, P5, P6, N5, (which is a push up stage), and other is formed by N7, N8, N9, N10, and P10, (which is a pull down stage). V_{UP} and $\overline{V_{DN}}$ are input control voltages. It does the normal charge pump operation, meaning that the output voltage, V_{out}, will work under three states, 00, 01, and 10, named as PFD output states. And the other stage use two control signals V_{DN} and $\overline{V_{UP}}$, to decrease the hold time of the state 11 so that we can get a shorter dead zone time and further improve the phase noise of frequency synthesizer.

To further reduce the lock time we adopt a similar technique[7] of adaptive band-width controller in our design. In the charge pump Fig. 7, the charge current is controlled by V_B, which is the gate voltage of N1 and N6. If we can dynamically control this voltage and thus can change the charge current then we can get a faster locked condition. Fig. 8 shows the circuit of our adaptive band-width controller. Circuit in Fig. 8(a) operates for two signals V_{UP} and V_{DN}, which are produced by PFD, to get a $\Delta\theta$ signal. When reference frequency and oscillator frequency are different from the logic level, the $\Delta\theta$ signal should be high. If $\Delta\theta$ is high then P3 and P5, shown in Fig. 8(b), will be ON and OFF, respectively; and there exist a charge path through P3 from V_{DD} to C_{BW}. Therefore, the control voltage V_B will increase and that in turn will increase the charge current to the charge pump. On an opposite to that, if $\Delta\theta$ is low then P3 and P5 will be OFF and ON, respectively; and there exist a discharge path through P5 from V_B to R_{BW}. This will decrease the control voltage V_B and that in turn will decrease the charge current through the charge pump. Moreover, the P5 guarantees that V_B is no less than V_{th}. Thus the charge current of charge pump will at least keep a minimum value.

4. SIMULATION RESULTS

The Phase noise is shown in Fig. 9, which is -123 dBc/Hz

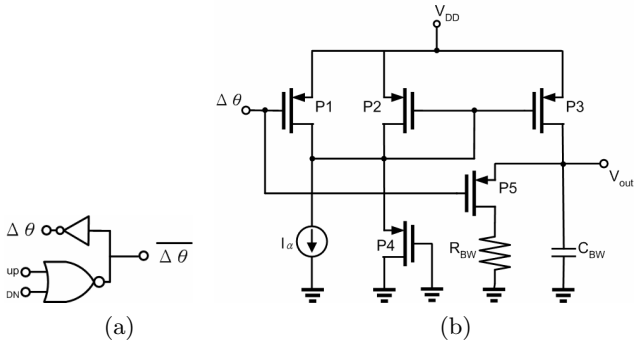

Figure 8: (a) control signal generator, (b) adaptive bandwidth controller

at 1MHz offset and KVCO is shown in Fig. 10, which is 1GHz/V. The charge pump and adaptive band width controller's waveform are shown in Fig. 11 and Fig. 12, respectively. VCO's transient simulation is shown in Fig. 13.

Test measurements were performed on the VCO that has separately been fabricated. Measurement shows a 10-15% deviation from the expected results. Keeping this in mind, a slightly different value for tuning circuit of VCO has been chosen in synthesizer design. Measured phase noise (Fig. 14) of the free running VCO at an offset of 1MHz is about -110 dBc. Measured tuning range of the VCO is shown in Fig.15. Die photo of VCO is shown in Fig.16, and finally, Frequency Synthesizer's layout is shown in Fig. 17.

5. CONCLUSION

A fully integrated PLL-based frequency synthesizer for the 802.11a/b/g wireless LAN applications is presented using 0.18um CMOS technology. The proposed design targets to improve performance and reduce power consumption by using a lower supply voltage. The performance of the proposed synthesizer is summarized in TABLE I.

Table 1: Summary of the performance

Technology		0.18μm mixed-signal CMOS
Voltage Supply		1-Volt
Reference Frequency		18.75MHz/20MHz
Output Frequency		2.4-2.7GHz/ 5.18-5.8275GHz
Channel Spacing		9.375MHz/20.33MHz
Power Dissipation	VCO	3.23mW
	Divider	2.7mW
	PFD+CP	1.1mW
	Total	7.03mW
Phase noise		-101 dBc/Hz@100KHz -123 dBc/Hz@1MHz
sidebands		-80dBc
Settling time(80MHz jump)		60μs@20ppm

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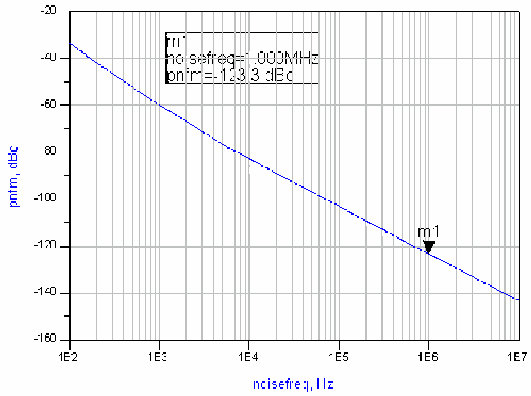

Figure 9: Phase noise of the VCO

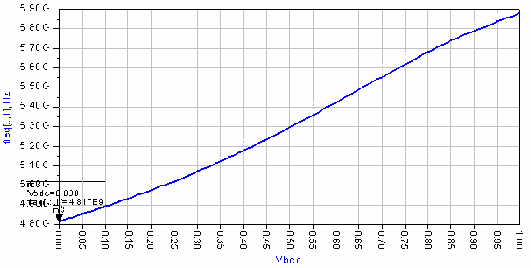

Figure 10: Tuning Range of the VCO

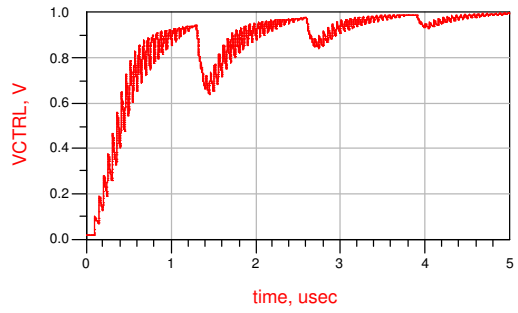

Figure 11: Charge Pump Waveform

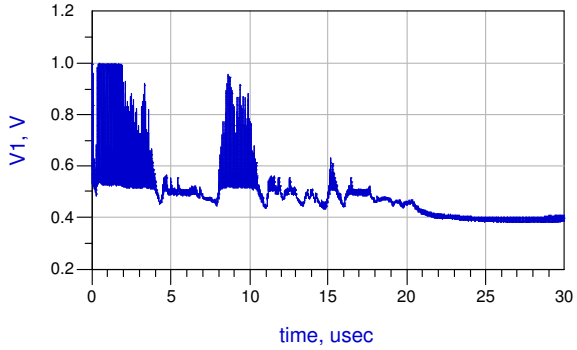

Figure 12: Adaptive Band-width Controller Waveform

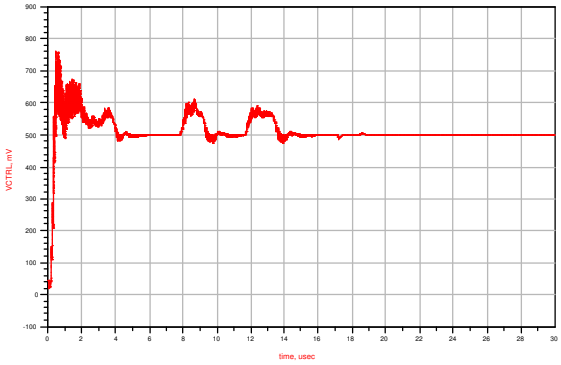

Figure 13: VCO Transient Simulation

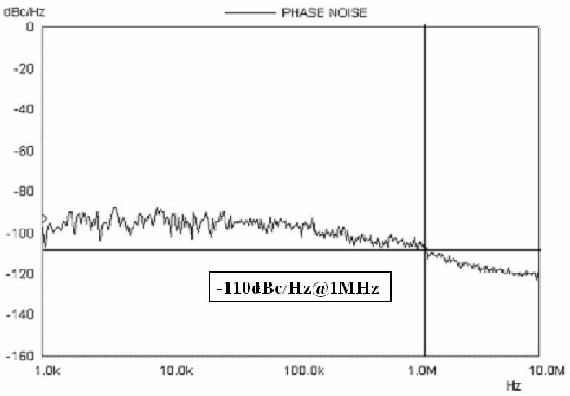

Figure 14: VCO measured Phase noise

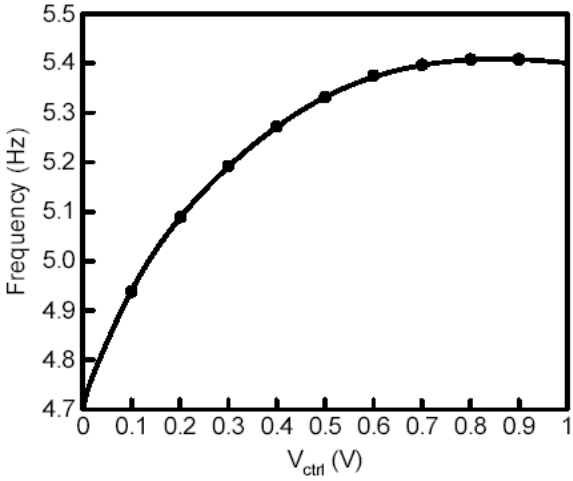

Figure 15: Measured tuning range of the VCO

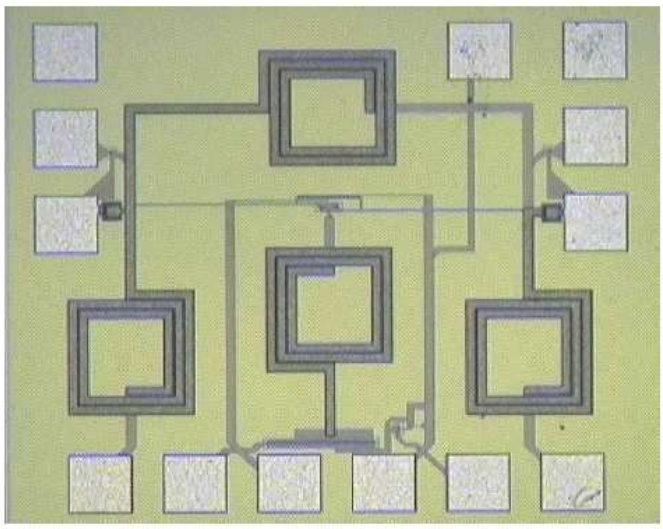

Figure 16: Die Photograph of VCO

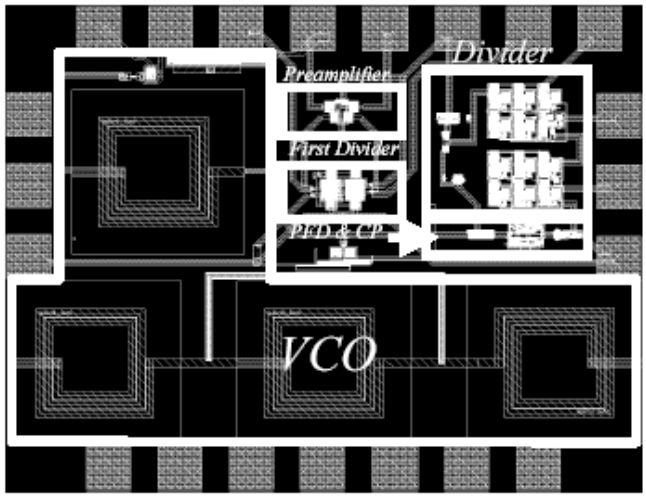

Figure 17: Layout of the Frequency Synthesizer