SCORE: SPICE COmpatible Reluctance Extraction[*]

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Abstract

Presently, a necessary modification to mainstream analysis tools prevents the direct application of reluctance k. In this paper, we propose a reluctance realization algorithm (RRA) by directly converting reluctances to circuit elements compatible with general simulation engines, such as SPICE. Reluctance realization is applicable to arbitrary circuit topology and no accuracy penalty is involved in the realization process. Since the stability of the converted circuit largely depends on the stability of the reluctance matrix, we present an efficient Improved Recursive Bisection Cutting Algorithm (IRBCA) to obtain stability-guaranteed reluctance matrices, and integrate IRBCA and RRA into a SPICE compatible reluctance extraction tool, SCORE.

1 Introduction

As VLSI technology advances into Ultra Deep Sub-Micron (UDSM) era and the operating frequency approaches multi-giga hertz range, efficient modeling of inductive effects becomes an indispensable issue, not only for IC packages but also for on-chip interconnects. The challenge of inductance modeling and analysis is discussed in [1, 5, 6].

One major problem of inductance modeling is the uncertainty of the current return path, which is unknown prior to parasitic extraction and circuit model simulation. Rosa [11] introduces the concept of partial inductance by assuming that each conductor segment has a current return path at infinity. Ruehli brings this concept to modern ICs and proposes the partial element equivalent circuit (PEEC) model [12, 13] to handle general three dimensional interconnects. FastHenry [9] speeds up the extraction process by multipole expansion.

Nonetheless, since inductance is a long-range effect that couples together many individual lines of multi-conductor interconnect, the PEEC model leads to an extremely dense inductance matrix $\mathcal{L}$ and can dramatically increase both model size and simulation runtime.

Various sparsification techniques of $\mathcal{L}$ have been introduced to alleviate this problem. The most straight forward way is to truncate small mutual inductance terms. As tempting as it may be, direct truncation results in loss of passivity and leads to an unstable system [7]. Krauter proposes the shift-and-truncate method [10], which assumes that the current return path is no longer at infinity but within a shell. However, complicated iterations is involved when trying to determine a proper shell radius to ensure desired accuracy. Other methods, such as the return-limited loop inductance method [14] and the block diagonal method [6], also reduce the number of mutual inductances by limiting the current return path to the nearest same-direction power-ground lines. However, they are inaccurate in practice when the order of dimension of power-ground lines is same as that of signal lines.

Recently, Hao Ji *et al.* [4] propose to sparsify on the reluctance matrix $\mathcal{K}$ (the inverse inductance matrix) instead of $\mathcal{L}$. Since reluctance has higher degree of locality similar to capacitance, only a small number of neighbors need to be considered. Therefore, $\mathcal{K}$ for circuit simulation is very sparse compared to $\mathcal{L}$. Furthermore, the reluctance-based method is numerically stable, since $\mathcal{K}$ is strictly diagonal dominant and all off diagonal terms are negative, which can be safely deleted without sacrificing stability. However, there are still some issues with the existing reluctance handling flow, albeit its great efficiency and accuracy in modeling inductive effects.

First, after reluctance extraction, circuit simulation is required to verify the signal integrity issue. Unfortunately, traditional circuit analysis tools cannot handle reluctance directly. [3] and [8] incorporate the capability to simulate reluctance, but significant modifications to traditional analysis tools are inevitable. Therefore, several previous works have dealt with generating SPICE compatible reluctance models. Beattie *et al.* [2] propose to do extra inversion of $\mathcal{K}$ to avoid simulating reluctance, however, the execution time is compromised by the double inversion of the matrix. Wire duplication [16] is used to construct a complexity-reduced

[*]This work is partially supported by National Science Council of Taiwan, R.O.C., under Grant NSC 92-2218-E-002-030.

1530-1591/04 $20.00 (c) 2004 IEEE

circuit that is equivalent to the circuit under the $\mathcal{L}$ matrix or under the truncated $\mathcal{K}$ matrix. However, it introduces lots of dummy wires and hence dramatically increases the circuit size. Yu *et al.* [15] present the vector potential equivalent circuit (VPEC) model which uses an effective resistance, called equivalent magnetic resistance (EMR) to model the mutual inductive coupling. But it requires extra steps to calculate EMR matrix after obtaining $\mathcal{K}$.

Second, [3] discovers that sufficient discretization of conductors in general interconnect configurations is necessary to guarantee that the reluctance matrix does not include positive off diagonal terms, which can seriously imperil the stability of reluctance-based methods. Recursive Bisection Cutting Algorithm (RBCA) is proposed to cut the longest wire in a small window when some entries in the reluctance matrix have positive values. However, the iterative inversion of $\mathcal{L}$ is time consuming.

In this paper, we present a reluctance realization algorithm, *RRA*, which directly converts reluctance to a mathematically and electrically equivalent circuit model, which only contains self inductances and VCVSs, and hence avoids modifications to mainstream analysis tools to simulate reluctance. We will compare *RRA* with other existing SPICE compatible reluctance models in detail. Furthermore, we improve RBCA to guarantee the stability by proposing that cutting wires should be based on their coupling magnitude instead of length. A SPICE compatible reluctance extraction tool, *SCORE*, is presented by integrating *RRA* with *IRBCA*.

The rest of paper is organized as follows: Section 2 introduces the reluctance realization algorithm. Section 3 presents *IRBCA* and the algorithm flow of *SCORE*. Simulation results are presented in Section 4. The paper is concluded in Section 5.

2 Reluctance Realization

In this section, we present the reluctance realization algorithm. A detailed algorithm flow is given at the end of this section.

2.1 Notations and Assumptions

We first define some notations that we will use throughout this paper. Our discussion is applicable to RLKC-VJ[1] circuits with arbitrary topology.

- Given a circuit, the total number of nodes is denoted by N and n_i denotes the i^{th} labeled node. The node voltage of n_i is v_i. Γ_i denotes the neighbor node set of n_i. The voltage drop between n_i and n_j is given by v_{ij}. i_{ij} is the total current flowing from n_i to n_j.
- y_{ij} represents the total admittance between n_i and n_j. k_{ij} denotes the self reluctance between n_i and n_j. M_{ij} stands for the coupling set of k_{ij}, which means that if $k_{mn} \in M_{ij}$, a mutual reluctance, k_{mn}^{ij}, exists between k_{ij} and k_{mn}.

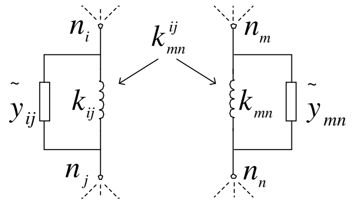

Figure 1. Notations.

Fig. 1 illustrates some of the introduced notations. Dash lines represent connections to other nodes.

2.2 Derivation

Given a linear circuit, the MNA formulation can be expressed as follows:

$$\widetilde{G}X + s\widetilde{C}X = B \tag{1}$$

in which

$$\widetilde{G} = \begin{bmatrix} G & A_l^T \\ -A_l & 0 \end{bmatrix}, \quad \widetilde{C} = \begin{bmatrix} C & 0 \\ 0 & L \end{bmatrix}$$
$$X = \begin{bmatrix} V_n \\ I_l \end{bmatrix}, \quad B = \begin{bmatrix} -A_i^T I_s \\ 0 \end{bmatrix} \tag{2}$$

$G = A_g^T \mathcal{G} A_g$ and $C = A_c^T \mathcal{C} A_c$. $\mathcal{G}$, $\mathcal{C}$, and $\mathcal{L}$ are conductance, capacitance, and inductance matrices respectively. A's are the adjacency matrices of the circuit, whose subscriptions g, c, l, and i associate with $\mathcal{G}$, $\mathcal{C}$, $\mathcal{L}$ and I_s respectively. I_s is the vector of independent current sources. V_n and I_l are vectors of node voltage and inductance current variables.

From Eq. 1 and 2, we obtain that:

$$YV_n = (G + sC + \frac{1}{s}K)V_n = J \tag{3}$$

in which $K = A_k^T \mathcal{K} A_k$ and $J = -A_i^T I_s$. $\mathcal{K}$ is the reluctance matrix and A_k is the adjacency matrix of $\mathcal{K}$. obtain: Therefore, the admittance matrix Y of the given circuit can be decomposed into two parts: $\widetilde{Y}$ and K, where $\widetilde{Y} = G + sC$. Let $\widetilde{V} = KV_n$, Eq. 3 can be expressed as:

$$\widetilde{Y}V_n + \frac{1}{s}\widetilde{V} = J \tag{4}$$

[1] An RLKC-VJ circuit contains resistances (conductances), inductances, reluctances, capacitances, independent voltage and current sources.

where $\widetilde{V}$ is called the *concocted voltage drop vector*.

Suppose that n_i and n_j are neighbor nodes as shown in Fig. 1. Coefficients in the i^{th} and j^{th} row of set of equations represented by 4 are coefficients of the nodal equations for n_i and n_j, respectively:

$$\sum_{\forall n_k \in \Gamma_i} \widetilde{y}_{ik} v_{ik} + \frac{1}{s}\widetilde{v}_i = j_i \quad (5)$$

$$\sum_{\forall n_k \in \Gamma_j} \widetilde{y}_{jk} v_{jk} + \frac{1}{s}\widetilde{v}_j = j_j \quad (6)$$

where $\widetilde{v}_i$ and $\widetilde{v}_j$ are the i^{th} and j^{th} term in $\widetilde{V}$.

The following two equations can be obtained from the definition of *concocted voltage drop vector*, $\widetilde{V} = KV_n$:

$$\widetilde{v}_i = \sum_{\forall n_k \in \Gamma_i} (k_{ik} v_{ik} + \sum_{\forall k_{pq} \in M_{ik}} k_{pq}^{ik} V_{pq}) = \sum_{\forall n_k \in \Gamma_i} \widetilde{v}_{ik}$$

$$\widetilde{v}_j = \sum_{\forall n_k \in \Gamma_j} (k_{jk} v_{jk} + \sum_{\forall k_{pq} \in M_{jk}} k_{pq}^{jk} V_{pq}) = \sum_{\forall n_k \in \Gamma_j} \widetilde{v}_{jk}$$

From the above two equations, we conclude that if k_{ij} exists between node n_i and n_j, contributions of k_{ij} and mutual reluctances in its coupling set M_{ij} to $\widetilde{v}_i$ and $\widetilde{v}_j$ are given by:

$$\widetilde{v}_{ij} = k_{ij} v_{ij} + \sum_{\forall k_{pq} \in M_{ij}} k_{pq}^{ij} v_{pq} \quad (7)$$

$$\widetilde{v}_{ji} = k_{ij} v_{ji} + \sum_{\forall k_{pq} \in M_{ij}} k_{pq}^{ji} v_{pq} \quad (8)$$

The above two equations lead to the following relation:

$$\widetilde{v}_{ij} = -\widetilde{v}_{ji} \quad (9)$$

The total current I_{ij} flowing out of n_i and across the connection between n_i and n_j is:

$$i_{ij} = \widetilde{y}_{ij} v_{ij} + \frac{1}{s}\widetilde{v}_{ij} = \widetilde{y}_{ij} v_{ij} + \frac{1}{s}[v_i - (v_i - \widetilde{v}_{ij})] \quad (10)$$

$1/s$ on the right hand side of Eq. 10 can be viewed as the admittance of a one-Henry inductance, which connects node n_i and a *concocted node*, n_{ci}. The node voltage of n_{ci} is $v_i - \widetilde{v}_{ij}$. Therefore, the current i_{ij} consists of two parts: one flows through $\widetilde{y}_{ij}$ to n_j; another flows through a one-Henry inductance to n_{ci}, which is shown in Fig. 2. The voltage drop on the inductance is $\widetilde{v}_{ij}$.

Likewise, by applying Eq. 7, the current i_{ji} flowing from n_j to n_i is given by:

$$i_{ji} = \widetilde{y}_{ij} v_{ji} + \frac{1}{s}\widetilde{v}_{ji} = \widetilde{y}_{ij} v_{ji} + \frac{1}{s}[v_j - (v_j + \widetilde{v}_{ij})] \quad (11)$$

It also consists of two parts: one flows through $\widetilde{y}_{ij}$ to n_i; another flows across a one-Henry inductance to another *concocted node* n_{cj} of node voltage $v_j + \widetilde{v}_{ij}$.

Similar relations can be obtained for the current flowing between n_m and n_n. Hence, the circuit in Fig. 1 is equivalent with the one shown in Fig. 2.

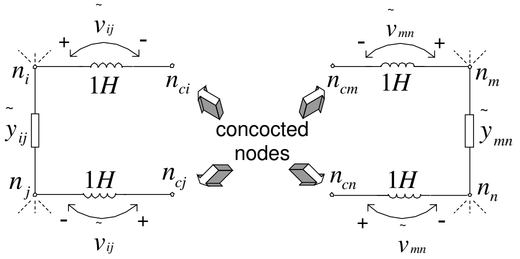

Figure 2. Concocted nodes.

Node voltages of n_{ci} and n_{cj} are $v_i - \widetilde{v}_{ij}$ and $v_j + \widetilde{v}_{ij}$, respectively. By applying Eq. 7 and 8, the voltage drop $v_{ci,cj}$ between concocted nodes n_{ci} and n_{cj} is obtained as:

$$v_{ci,cj} = V_{ij} - 2\widetilde{v}_{ij} = (1 - 2k_{ij})v_{ij} - \sum_{\forall k_{pq} \in M_{ij}} 2k_{pq}^{ij} v_{pq}$$

From the above equation, one can see that several serially connected VCVSs can be connected between n_{ci} and n_{cj} to guarantee that the node voltage of n_{ci} is $v_i - \widetilde{v}_{ij}$ and the node voltage of n_{cj} is $v_j + \widetilde{v}_{ij}$, as shown in Fig. 3. In Fig. 3, reluctances have been replaced by SPICE compatible circuit elements.

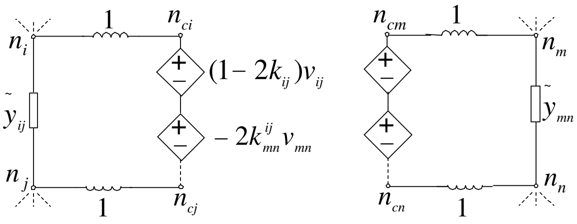

Figure 3. VCVSs to maintain branch currents.

However, the circuit in Fig. 3 is not in a simplified form. First, serial inductances can be combined to reduce element number. Furthermore, we notice that the new branch including inductances and VCVSs can be simplified to the one shown in Fig. 4.(b). Applying a port voltage v_{ij} for circuits in Fig. 4.(a) and (b), it can be verified that their port currents are exactly same. However, the simplified branch in Fig. 4.(b) has one less VCVS.

After simplification, the branch shown in Fig. 4.(b) is our equivalent circuit model to replace k_{ij}. This SPICE compatible model includes a $1/k_{ij}$ Henry inductance and multiple serial VCVSs. The number of VCVSs is determined by the number of elements in M_{ij}, which is the coupling set of k_{ij}.

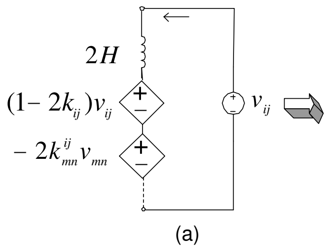

Figure 4. Simplified branch.

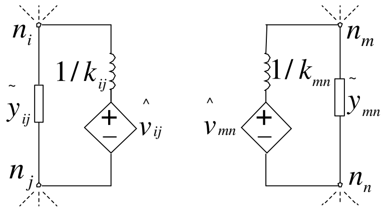

Figure 5. Reluctance realization.

Fig. 5 shows the circuit after replacing reluctances in Fig. 1. $\widehat{v}_{ij}$ and $\widehat{v}_{mn}$ in Fig. 5 are called *composite VCVS*, which is the combination of connected VCVSs.

$$\begin{aligned}\widehat{v}_{ij} &= -\sum_{\forall k_{pq}\in M_{ij}} \frac{k_{pq}^{ij}}{k_{ij}} v_{pq} \\ \widehat{v}_{mn} &= -\sum_{\forall k_{pq}\in M_{mn}} \frac{k_{pq}^{mn}}{k_{mn}} v_{pq}\end{aligned}$$

The circuit in Fig. 5 is mathematically and electrically equivalent to the one in Fig. 1. However, the final circuit only includes SPICE compatible circuit elements.

2.3 Algorithm Flow

The detailed reluctance realization algorithm is presented in Table 1. It can be either combined into an extraction tool or programmed as post-extraction software.

```
For each node $n_i$ in a given circuit including reluctances
 I.For each unmarked neighbor node $n_j$ in $\Gamma_i$
  1.Output circuit elements except reluctances
  2.If self reluctance $k_{ij}$ exits
    a.let $n_{ci}^q$=$n_i$
    b.For each $k_{mn} \in M_{ij}$
     Output VCVS $-k_{mn}^{ij}/k_{ij}V_{mn}$ between $n_{ci}^q$ and $n_{ci}^{q+1}$
     q=q+1.
    c.Output inductance $1/k_{ij}$ between $n_{ci}^q$ and $n_j$.
 II.Mark $n_i$
```

Table 1. Reluctance Realization Algorithm.

Our *RRA* has many advantages over existing SPICE compatible reluctance-based methods. Double inversion [2] method needs to do extra inversion of $\mathcal{K}$ and VPEC [15] takes two additional steps to calculate $\widehat{G}$ and EMR matrix, $\widehat{R}$, after $\mathcal{K}$ is obtained, while *RRA* directly converts reluctances to SPICE compatible circuit elements without extra efforts. Another advantage of *RRA* is that it generates SPICE compatible circuit model in spite of the passivity of $\mathcal{K}$. However, VPEC requires a positive definite $\mathcal{K}$ to obtain equivalent magnetic resistances with positive values. Compared to wire duplication [16], *RRA* results in much smaller circuit size, since it only requires two VCVSs to represent a mutual reluctance. However, wire duplication needs four times couplings as required in $\mathcal{K}$. Reluctance realization is discussed further in Section 4.

3 Improved RBCA

The stability of the converted circuit depends largely on the stability of the reluctance matrix. Therefore, a stable reluctance matrix is important to *SCORE*.

In [3], it's discovered that in general interconnect configurations, the reluctance matrix obtained by directly inverting the partial inductance matrix may include positive off diagonal terms, which seriously imperil the stability of the K method.

An example $\mathcal{L}$ matrix from [3] is given by:

$$L=\begin{bmatrix} 1.04 & 0.34 & 0.37 & 0.24 & 0.51 \\ 0.34 & 0.45 & 0.09 & 0.06 & 0.27 \\ 0.37 & 0.09 & 1.04 & 0.34 & 0.41 \\ 0.24 & 0.06 & 0.34 & 0.45 & 0.11 \\ 0.51 & 0.27 & 0.41 & 0.11 & 1.69 \end{bmatrix} \times 10^{-10} H$$

The reluctance matrix $\mathcal{K}$ by inverting $\mathcal{L}$ is:

$$K=\begin{bmatrix} 1.57 & -0.94 & -0.22 & -0.47 & -0.25 \\ -0.94 & 3.02 & 0.15 & 0.01 & -0.23 \\ -0.22 & 0.15 & 1.42 & -0.93 & -0.24 \\ -0.47 & 0.01 & -0.93 & 3.12 & 0.16 \\ -0.25 & -0.23 & -0.24 & 0.16 & -0.75 \end{bmatrix} \times 10^{-10} H$$

Obviously some off diagonal entries in the reluctance matrix are positive. And hence eigenvalues of the reluctance matrix are not guaranteed to lie in the right hand side of the complex plane.

It has been shown that the unstable reluctance matrix is caused by *insufficient discretization* [3]. Therefore, the stability can be guaranteed by finer discretized conductors. The proposed RBCA cuts the longest wire in a small window in case that the small reluctance matrix has positive off diagonal terms.

Suppose that the coupling between conductors i and j is represented by $[i, j]$ and the magnitude of $[i, j]$ is the value of entry (i, j) in $\mathcal{L}$. We observe that positive entries in the reluctance matrix are mainly caused by the following two situations:

1. *Given conductors i, j, and k, if couplings $[i, k]$ and $[j, k]$ are strong, while the coupling $[i, j]$ is weak, positive off diagonal values may exist in entries (i, j) and (j, i) of the reluctance matrix.*
2. *Given conductors i, j, and k, if couplings $[i, j]$ and $[i, k]$ are weak, while the coupling $[j, k]$ is strong, positive off diagonal values may exist in entries (i, k) and (k, i) of the reluctance matrix.*

Therefore, *it's more reasonable to cut conductors based on coupling magnitude instead of length*. In the first situation, instead of cutting the longest wire as proposed by RBCA, we cut conductor k, since cutting k decreases couplings $[i, k]$ and $[j, k]$. While in the second situation, we select to cut conductor j, because it weakens couplings $[i, j]$ and $[j, k]$.

Suppose in the above example, conductors are numbered from 1 to 5 in terms of their row numbers in $\mathcal{L}$. In the first situation, assume that the aggressor is conductor 3. The current in 3 induces opposite direction currents in other conductors. Since the coupling $[3, 1]$ is much stronger than that between 3 and 2, the induced current in 2 is smaller than the induced current in 1. However, the induced current in 1 also induces another current in conductor 2. This induced current has the same direction as the current in the aggressor. Because the coupling between 1 and 2 is strong, the overall current in conductor 2 may be in the positive direction. Hence entries (3,2) and (2,3) in $\mathcal{K}$ have positive values. According to the first situation, conductor 1 will be cut, since the positive induced current in conductor 2 decreases when couplings $[3, 1]$ and $[1, 2]$ are weakened.

Positive entries (2,4) and (4,2) in the reluctance matrix can be explained by the second situation. Suppose that the aggressor is conductor 2. The current in 2 induces small currents in conductor 3 and 4 in that couplings $[2, 3]$ and $[2, 4]$ are weak. However, the coupling $[3, 4]$ is strong, and hence in conductor 4, the current induced by conductor 3 may be larger than the current induced by 2. The overall effect is that the current induced in 4 has the same direction as the current in 2. Therefore, entries (2,4) and (4,2) are positive. In this case, conductor 3 will be bisected to decrease couplings $[2, 3]$ and $[3, 4]$.

In the extraction process, we first calculate the partial inductance matrix in a small window. Then we set a scalar T. Couplings between different conductors are examined in the partial inductance matrix. If strong couplings are T times larger than weak couplings, suitable conductors are selected to be bisected in terms of the above two situations, and the small $\mathcal{L}$ matrix is recalculated. Then we calculate the corresponding reluctance matrix. The value of T is dynamically adjusted during the extraction flow. After obtaining the reluctance matrix, its off diagonal entries are checked to ensure that they all have negative values. If some positive values still exist, we adjust T to a smaller value and reexamine the coupling relation in the partial inductance matrix; otherwise, T is set to a larger value to avoid unnecessary cutting. Table 2 gives the algorithm flow of *SCORE*, which combines *IRBCA* with *RRA*.

```
For each conductor j
  1. Choose a window $W$.
  2. Calculate the partial inductance matrix $\mathcal{L}$ of a small
     structure enclosed in $W$.
  3. Calculate the small $\mathcal{K}$ matrix as in the K method.
  4. If $\exists \mathcal{K}_{ij} > 0$, $i \neq j$, do the following:
    a. check coupling relation and select troublemaker
       conductors to be cut.
    b. Backtrace and reperform the small matrix inversion.
       If this cutting causes any new positive off diagonal
       terms, recursively perform the cutting process.
  5. Reluctance realization.
```

Table 2. Algorithm flow of SCORE.

4 Experimental Results

In this section, we use a few examples to show the efficiency and accuracy of *SCORE*. We implement *SCORE* in C language. All tests are run on a PIII 900MHz machine with 256MB memory.

The testing conductor system is a portion of conductors in metal 7 layer. It contains 218 conductor segments. All segments have different lengths, but identical width, which is $0.6\mu m$. A $1v$ step input is applied at one end of a conductor segment and we measure its transient voltage response at the far end.

First, we compare simulation results of different extraction methods by applying *SCORE*, full L, K method, double inversion, and direct truncation. Circuits including reluctances are simulated by InductWise [3]. Taking full L as the reference waveform, it can be seen from Fig. 6 that *SCORE* and the K method have higher accuracy than the other methods. It's not surprising that waveforms of *SCORE* and the K method are quite close, since they have mathematically equivalent circuit models. The small difference is partially caused by the use of different simulators.

SPICE simulation times for full L, *SCORE,* and double inversion are listed in the Table 4. The truncation method is neglected, since it cannot guarantee the stability. For this testing conductor system, *SCORE* demonstrates about $528x$ speedup over full L extraction.

As one can see from Section II, the reluctance realization process introduces additional nodes and different circuit elements. Therefore, we need to measure the simula-

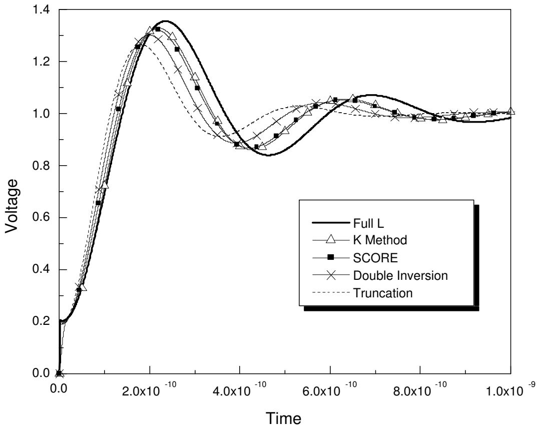

Figure 6. Simulation waveforms.

Extraction Method	Simulation Time	Speedup
Full L	29520.1s	1x
SCORE	55.9s	528x
Double Inversion	436.1s	67.7x

Table 3. SPICE simulation time.

tion time overhead. Since SPICE cannot handle reluctances, we implement the reluctance realization algorithm as an individual program and use InductWise to simulate extracted circuits before and after conversion. To compare fairly, the whole conductor system containing 28,048 segments in metal 5-7 is used for testing. Extraction takes about 368 seconds and *RRA* uses 8 seconds to generate SPICE compatible circuit. Simulation results demonstrate about 23% simulation time overhead after reluctance realization. However, *SCORE* generates SPICE compatible circuits that can be directly fed into general analysis tools.

From the above experimental results, *SCORE* demonstrates the best compromise between accuracy and efficiency. It has the shortest SPICE simulation time, while maintaining the same accuracy as the K method.

5 Conclusions

In this paper, we presented a SPICE compatible parasitic extraction tool, *SCORE*. *SCORE* integrates reluctance realization algorithm, *RRA*, with Improved Recursive Bisection Cutting Algorithm, *IRBCA*.

The K element realization algorithm converts a reluctance to a circuit model containing an inductance and serially connected VCVSs. They are mathematically equivalent. Since inductances and VCVSs can be handled by general analysis tools, modifications on those tools to handle reluctances are avoided. *IRBCA* is proposed to guarantee the stability of the reluctance matrix, and hence ensures the stability of the extracted circuit.

Experimental results demonstrate that *SCORE* has the best compromise between accuracy and efficiency compared to other SPICE compatible methods. It has the shortest SPICE simulation time, while maintaining the same accuracy as the K method.

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