Realizable Reduction for Electromagnetically Coupled $RLMC$ Interconnects*

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Abstract

This paper presents a realizable $RLMC$[1] reduction algorithm for extracted interconnect circuits based on two effective approaches: RL branch reduction and RC/LC node reduction. Our algorithm takes advantage of some structures existing extensively in interconnect circuits and hence has extremely fast execution time. It takes about 8 seconds to reduce a circuit of over 300,000 elements while maintaining 3% error and 75% element reduction ratio.

1 Introduction

Generally, an extracted $RLMC$ interconnect circuit consists of pure capacitance branches, pure resistance branches, and serially connected resistance and inductance branches (RL *branches*). Except for the internal nodes in RL branches, most floating nodes are connected to grounded or coupling capacitances.

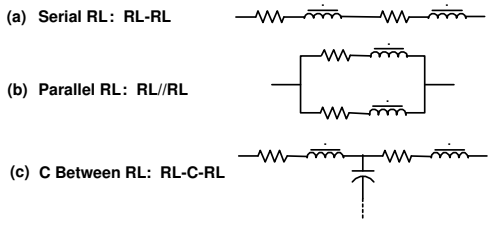

Figure 1. Common Structures

Fig. 1 shows some common structures in interconnect circuits. Since extraction tools extensively use RL branches to model interconnect segments, statistically, they may account for 60%-70% or even more of the circuit size. Therefore, it's our motivation to devise a fast reduction algorithm that takes advantage of those structures [1].

Our reduction procedure consists mainly of two stages: *RL branch reduction* and *RC/LC node reduction*. In the *RL branch reduction* stage, we first combine multiple serial RL branches or parallel RL branches shown in Fig. 1 into one RL branch. After this step, most nodes will have two RL branches and capacitances on them shown in the last structure in Fig. 1. Those coupling or grounded capacitances impede us from further reducing RL branches. Therefore, we propose *capacitance splitting* method to divide and shift the internal grounded and coupling capacitances to outside nodes, even when multiple capacitances exist. After splitting and shifting capacitances, the serial RL branches can be combined into one.

In the *RC/LC node reduction* stage, we first apply *element swapping* to obtain pure RC nodes or pure LC nodes. RC nodes can be eliminated by applying existing RC reduction algorithms. For LC nodes, we apply *capacitance splitting* similar to the technology applied in the *RL branch reduction* stage to obtain serial inductances, which can be easily reduced thereafter. Based on these approaches, we present a high-level reduction algorithm in the following table.

Algorithm: Realizable $RLMC$ Reduction
I. RL branch reduction.
1. Combine serial and parallel RL branches.
2. If $RL - C - RL$ structures exist:
a. Capacitance splitting.
b. Combine serial RL branches.
II. RC/LC node reduction.
1. Elements Swapping.
2. For RC nodes, apply RC reduction.
3. For LC nodes:
a. Capacitance splitting.
b. Combine serial inductances.

Table 1. Realizable $RLMC$ Reduction

2 Reduction Methodology

In this section, we present our methods for RL branch reduction and RC/LC node reduction.

METHOD 1 *(Combine serial RL Branches) If the i^{th} and the j^{th} branch are in series, they can be combined into one RL branch. Denote the combined resistance and inductance as R_{join} and L_{join} respectively. Then $R_{join} =$*

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[1] R: resistance or conductance; L: self inductance; M: mutual inductance; C: capacitance.

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$R_1 + R_2$, $L_{join} = L_i + 2L_{ij} + L_j$, *and the mutual inductance between* L_{join} *and* L_k *is* $L_{join,k} = L_{ik} + L_{jk}$.

METHOD 2 *(Combine Parallel* RL *Branches) Given two* RL *branches* i *and* j *in parallel, if* $\frac{R_i}{R_j}$ *equals or approximates* $\frac{L_i - L_{ij}}{L_j - L_{ij}}$*, these two* RL *branches can be combined into one. The combined resistance and inductance are* $R_{join} = \frac{R_i R_j}{R_i + R_j}$ *and* $L_{join} = \frac{R_i^2 L_j + 2R_i R_j L_{ij} + R_j^2 L_i}{(R_i + R_j)^2}$*. The mutual inductance between* L_{join} *and* L_k *is given by* $L_{join,k} = \frac{R_i L_{jk} + R_j L_{ik}}{R_i + R_j}$.

METHOD 3 *(Split Capacitances Between RL Branches) Suppose a capacitance* C *exists between two* RL *branches* i *and* j *shown in Fig. 2.(a), if* $R_i R_j C \ll (L_i + 2L_{ij} + L_j)$*, capacitance C can be split into different capacitances on outside nodes:* $C_1 = \frac{R_j}{R_i + R_j} C$ *and* $C_2 = \frac{R_i}{R_i + R_j} C$.

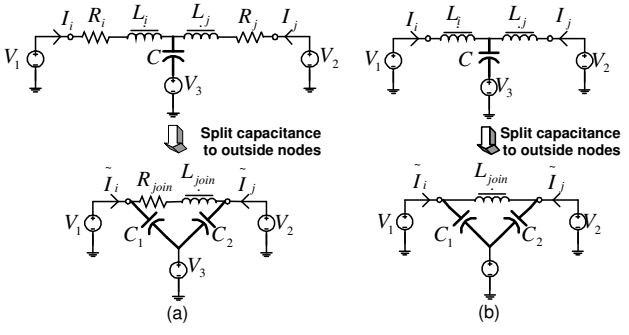

Figure 2. Split Capacitances.

In case that the RL reduction methods are not applicable, we show in Fig. 3 that by properly swapping some serially connected elements, pure RC nodes or pure LC nodes can be obtained.

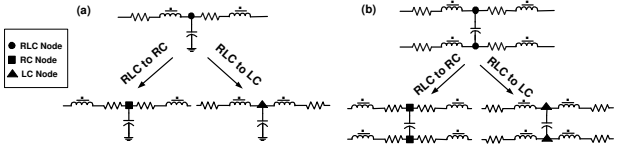

Figure 3. Elements Swapping.

METHOD 4 *(Split Capacitances on LC Nodes) If* $s^2(L_i + 2L_{ij} + L_i)C \ll 1$*, the capacitance on an* LC *node can be split to its neighboring nodes shown in Fig. 2.(b). The two divided capacitances are:* $C_1 \approx \frac{L_j + L_{ij}}{L_{join}} C$ *and* $C_2 \approx \frac{L_i + L_{ij}}{L_{join}} C$*, where* $L_{join} = L_i + 2L_{ij} + L_j$.

3 Experimental Results

Fig. 4 plots the waveforms of a testing circuit before and after reduction. This testing circuit is extracted from an interconnect system including 138 conductor segments. For this testing circuit, the maximum difference is less than $50mV$. Fig. 5 shows the detection of crosstalk by applying our $RLMC$ reduction algorithm. Fig. 6 plots the runtime and memory consumption for different circuits.

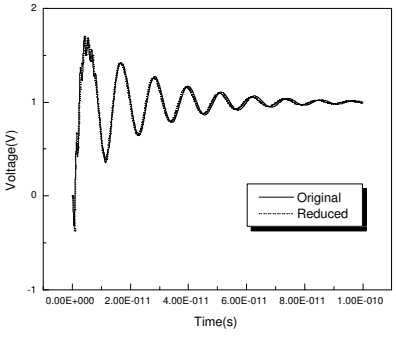

Figure 4. Waveforms Before/After Reduction

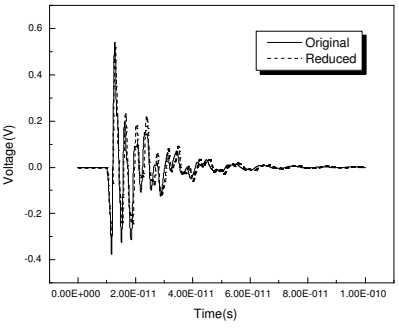

Figure 5. Crosstalk Detection

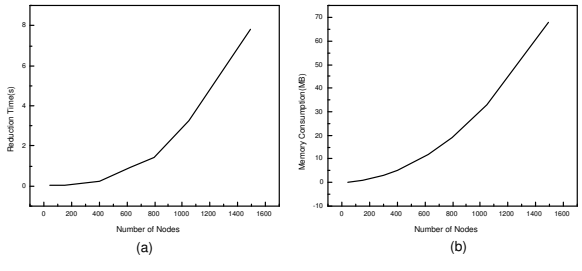

Figure 6. (a) Execution Time; (b) Memory Consumption.

For the testing circuit, it demonstrates that about 50% node reduction ratio and 72% element reduction ratio are achieved. However, one can adjust reduction conditions shown in previous methods to arrive at a better compromise between reduction ratio and accuracy.

References

[1] R. Jiang and C. C.-P. Chen. Realizable reduction for electromagnetically coupled rlmc interconnects. *EDA Group, University of Wisconsin, Madison*.