EPEEC: A Compact Reluctance Based Interconnect Model Considering Lossy Substrate Eddy Currents

Rong Jiang
Electrical and Computer Engineering
College of Engineering
University of Wisconsin, Madison, WI 53706

Charlie Chung-Ping Chen
Graduate Institute of Electronics Engineering
& Department of Electrical Engineering
National Taiwan University, Taipei 106, Taiwan

Abstract— **Lossy silicon substrate has significant effects on the already complicated interconnect modeling issue. To account for the substrate loss, traditional electromagnetic methods are often computationally prohibitive for large scale VLSI geometries. In this paper, we present EPEEC (Eddy-current-aware Partial Equivalent Element Circuit) which extends the traditional PEEC model to consider substrate eddy current loss based on complex image theory and skin and proximity effects by discretization of conductors. To deal with even larger scale of interconnects, we enhance EPEEC model to use reluctance by equipping it with an advanced windowing algorithm to further reduce the model size and runtime. Detail comparisons with state-of-the-art tools such as FastHenry and Momentum demonstrate that EPEEC is within 1% accuracy while providing over 100X speedup.**

I. Introduction

Due to the proliferation of mixed analog-digital system and radio frequency integrated circuit (RFIC), the development of efficient interconnect models for such a system is made difficult because of the lossy nature of the silicon substrate. In particular, the creation of eddy currents in the conductive silicon substrate can lead to significant interconnect inductance loss. An interconnect system analysis without considering the lossy substrate effect will result in an over-designed network and waste chip resources.

With the increasing clock frequency and integration density, intentional and unintentional inductance effects gradually rise. PEEC method [1] has been widely adopted to extract line parameters for on-chip interconnetcs. However, since PEEC model assumes current return paths at infinity, extremely dense partial inductance matrices are usually generated which dramatically increases both model size and simulation runtime. For this reason, various inductance sparsification techniques have been introduced to alleviate this problem [2]–[4]. In particular, the reluctance-based method [5] [6] has been proposed. Since reluctance has higher degree of locality similar to capacitance, only a small number of neighbors need to be considered, and hence reluctance matrix for circuit simulation is very sparse compared to partial inductance matrix.

Moreover, the traditional PEEC approach does not take the substrate loss effect into consideration and hence cannot capture the inductance loss due to the formation of eddy currents. Although several works have been proposed to resolve this issue by constructing three dimensional linear substrate models [7]–[9], most of these approaches employ a numerical finite difference based method by spatially discretizing a large volume of silicon bulk and hence will lead to equivalent circuits prohibitive in size.

In this paper, we propose an accurate and efficient method to extend the PEEC model to consider the substrate eddy current loss based on the complex image theory [10], which has been recently used in RFIC regime to accurately capture line impedances of microstrips [11]–[13] on lossy silicon substrates. Complex image theory generates interconnect models based on the configuration of substrate structure instead of discretizing the substrate and hence can result in very compact models for interconnects.

To deal with millions of interconnects and their images, we enhance the extended PEEC model to use reluctance element with an extended window searching reluctance extraction algorithm. Finally, since this new model, EPEEC, includes mutual resistances and reluctances, in order to be applicable to general circuit simulators, SPICE compatible models for mutual resistance and reluctance are also provided. Detail comparisons with state-of-the-art tools such as FastHenry and Momentum demonstrate that EPEEC is within 1% accuracy while providing over 100X speedup.

II. Substrate Eddy Current

Eddy current in the substrate is caused by time varying magnetic fields. If a time varying magnetic flux density $\mathbf{B}_f$ is induced in the substrate by currents in interconnects, an electric field $\mathbf{E}$ is produced:

$$\bigtriangledown \times \mathbf{E} = -\frac{\partial \mathbf{B}_f}{\partial t} \tag{1}$$

The electric field $\mathbf{E}$ can be expressed in terms of the vector magnetic potential $\mathbf{A}$ by:

$$\mathbf{E} \;=\; -\frac{\partial \mathbf{A}}{\partial t} \tag{2}$$

This electric field in turn establishes a current flowing according to the Ohm's law:

$$\mathbf{J} \;=\; \sigma \mathbf{E} \tag{3}$$

Substituting Eq. (3) into Eq. (2) leads to:

$$\mathbf{J} = -\sigma\frac{\partial \mathbf{A}}{\partial t} \tag{4}$$

Since these induced currents will produce another magnetic field according to Ampere's Law:

$$\bigtriangledown \times \mathbf{B} = \mu \mathbf{J} \tag{5}$$

By using the fact that the vectors $\mathbf{A}$, $\mathbf{J}$, and $\mathbf{B}$ are solenoidal, we get $\bigtriangledown \cdot \mathbf{A} = 0$, $\bigtriangledown \cdot \mathbf{J} = 0$, $\bigtriangledown \cdot \mathbf{B} = 0$. Applying the vector identity$\bigtriangledown \times (\bigtriangledown \times \mathbf{F}) = \bigtriangledown(\bigtriangledown \cdot \mathbf{F}) - \bigtriangledown^{2}\mathbf{F}$, we obtain:

$$\bigtriangledown^2 \mathbf{A} = -\mu \mathbf{J} \tag{6}$$

Substitute Eq. (4) into Eq. (6), we can obtain that:

$$\bigtriangledown^2 \mathbf{A} - \mu\sigma\frac{\partial \mathbf{A}}{\partial t} = 0 \tag{7}$$

Eq. (7) is the diffusion equation for the magnetic vector potential in a medium subject to a time varying magnetic field.

III. Complex Image Theory

For frequencies up to a few Giga Hertz, the wavelength of the magnetic fields far exceeds a typical die's dimension. Thus we can make magneto-quasi-static approximations. This implies that no charge accumulation on the surface of the substrate and interconnects, and hence currents will flow parallel to the horizontal plane.

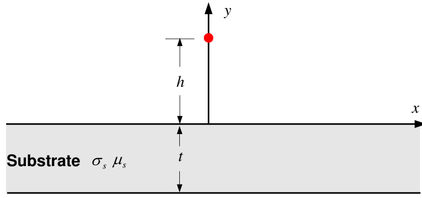

Fig. 1. Line Current Parallel to Substrate

Thus only the z-component of the vector potential exists and the problem becomes two dimensional. Since regions above and below the substrate have zero conductivity, from Eq. (7), we can obtain magnetic vector potential diffusion equations in different regions.

$$\begin{cases} \bigtriangledown^2 \mathbf{A}_t(x,y) = 0 & \text{Above Substrate} \\ \bigtriangledown^2 \mathbf{A}_s(x,y) = \mu_s\sigma_s\frac{\partial \mathbf{A}_s(x,y)}{\partial t} & \text{Within Substrate} \\ \bigtriangledown^2 \mathbf{A}_b(x,y) = 0 & \text{Below Substrate} \end{cases} \tag{8}$$

By applying the method of separation variables and noticing the symmetry of the fields with respect to the y axis, it can be shown that general solutions of Eqs. (8) are:

$$\begin{cases} \mathbf{A}_t(x,y) = \int_0^\infty \left[T'(k)e^{ky} + T''(k)e^{-ky}\right]cos(kx)dk \\ \mathbf{A}_s(x,y) = \int_0^\infty \left[S'(k)e^{qy} + S''(k)e^{-qy}\right]cos(kx)dk \\ \mathbf{A}_b(x,y) = \int_0^\infty B(k)e^{ky}cos(kx)dk \end{cases} \tag{9}$$

where

$$p = \sqrt{j\omega\mu_s\sigma_s} \qquad q = (k^2+p^2)^{1/2} \tag{10}$$

In the region $0 \le y \le h$, since $\mathbf{B} = \bigtriangledown \times \mathbf{A}$ and only the z component of the vector potentials exists, the x and y components of the magnetic flux density will be:

$$\begin{aligned} \mathbf{B}_{tx} &= \frac{\partial \mathbf{A}_t}{\partial y} = \int \left[T'e^{ky} - T''e^{-ky}\right]kcos(kx)dk \\ \mathbf{B}_{ty} &= -\frac{\partial \mathbf{A}_t}{\partial x} = \int \left[T'e^{ky} + T''e^{-ky}\right]ksin(kx)dk \end{aligned} \tag{11}$$

The first part of Eq. (11) containing the exponential factor e^{ky} corresponds to the field caused by the filament, while the second part containing the factor e^{-ky} corresponds to the field produced by the eddy currents.

From basic EM theory, the magnetic flux density caused by a current filament is given by:

$$\mathbf{B}_f(x,y) = \frac{\mu_1 I}{2\pi}\cdot\frac{1}{r} \tag{12}$$

where in this case $r = [x^2+(y-h)^2]^{1/2}$. And we can express its x and y components in converging Fourier integrals:

$$\begin{aligned} \mathbf{B}_{fx} &= \frac{\mu_1 I}{2\pi}\frac{y-h}{x^2+(y-h)^2} = \frac{\mu_1 I}{2\pi}\int e^{-k|y-h|}cos(kx)dk \\ \mathbf{B}_{fy} &= \frac{\mu_1 I}{2\pi}\frac{x}{x^2+(y-h)^2} = \frac{\mu_1 I}{2\pi}\int e^{-k|y-h|}sin(kx)dk \end{aligned} \tag{13}$$

Comparing Eqs. (13) with the first parts of the right hand sides of Eqs. (11), it follows that:

$$T'(k) = \frac{\mu_1 I}{2\pi}\frac{e^{-kh}}{k} \tag{14}$$

Substituting Eq. (14) into Eqs. (9) and noticing that for $y \rightarrow +\infty$, the field must vanish, $\mathbf{A}_t(x,y)$ can be written as:

$$\mathbf{A}_t(x,y) = \int (\frac{\mu_1 I}{2\pi}\frac{e^{-k|y-h|}}{k} + T''e^{-ky})cos(kx)dk \tag{15}$$

In order to determine other coefficients T'', S', S'', and B in Eqs. (9), we need to apply the boundary conditions at the medium interfaces:

- Boundary at $y = 0$

$$\mathbf{B}_{ty} = \mathbf{B}_{sy} \qquad and \qquad \frac{1}{\mu_0}\mathbf{B}_{tx} = \frac{1}{\mu_s}\mathbf{B}_{sx} \tag{16}$$

- Boundary at $y = -t$

$$\mathbf{B}_{sy} = \mathbf{B}_{by} \qquad and \qquad \frac{1}{\mu_s}\mathbf{B}_{sx} = \frac{1}{\mu_0}\mathbf{B}_{bx} \tag{17}$$

We interest in the solution of the region above substrate. After applying those boundary conditions, we have four unknowns and four boundary conditions, thus we can obtain that:

$$\mathbf{A}_t(x,y) = \frac{\mu_1 I}{2\pi}\int (\frac{e^{-k|y-h|}}{k} - Q(k)e^{kd}\frac{e^{-k(y+h+d)}}{k})cos(kx)dk \tag{18}$$

where:

$$\begin{aligned} C_1 &= \frac{\mu_0 q + \mu_s k}{\mu_0 q - \mu_s k}e^{2qt} \\ Q(k) &= \frac{\mu_0 q(C_1-1) - \mu_s k(C_1+1)}{\mu_0 q(C_1-1) + \mu_s k(C_1+1)} \end{aligned} \tag{19}$$

According to complex image theory, the first term in Eq.

(18) is due to the physical line current located at $y = h$. While the second term can be attributed to an image line current located at $y = -(h + d)$, if $Q(k)e^{kd}$ can be approximated by one. Expanding $Q(k)e^{kd}$ into Taylor series at $k = 0$ and ignoring high order terms, we obtain that this requirement is satisfied if

$$d = 2\frac{\mu_s tanh(pt)}{\mu_0 p} \quad (20)$$

where p is given by Eq. (10). Thus the eddy current effect in the lossy substrate can be replaced by an image current located at the complex distance $d + h$ below the substrate surface. Alternatively, an image ground plane can be placed at $d/2 + h$ below the physical current filament.

IV. Extended PEEC Model

For interconnects within metal layer i, which has a distance d_{Mi} above the substrate, the lossy silicon substrate effect can be approximated by placing a complex image plane below metal layer i at an effective complex distance, h^i_{eff}. If we denote the thickness of oxide and silicon bulk as h_{ox} and h_{si} respectively, by using Eq. (20), the effective complex distance of metal layer i is given by:

$$h^i_{eff} = d_{Mi} + h_{ox} + \frac{\mu_s tanh(ph_{si})}{\mu_0 p} \quad (21)$$

Since for every metal layer of the on-chip conductor system, only the first term d_{Mi} in Eq. (21) is different, a common complex image plane is shared by all metal layers. Based on the method of image, the common complex image plane can be substituted by image conductors which are at a distance $2h^i_{eff}$ below the physical conductors in metal layer i.

Besides the lossy substrate effect, as the frequency goes high, the current in a physical conductor is no longer evenly distributed, which leads to significant changes in resistance and inductance values. In order to obtain wide band accuracy, those effects, namely skin effect and proximity effect, also need to be modeled. For capturing both skin and proximity effects, conductors have to be discretized into filaments so as to account for the non-uniform distribution of current within conductors [14].

The extended PEEC model, which is shown in Fig. 2, is obtained by the application of complex image theory and the discretization of both the physical and image conductors into filaments.

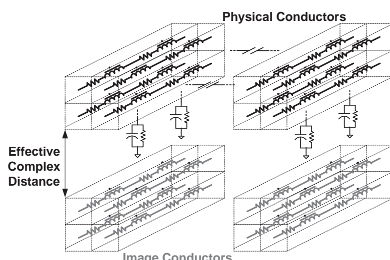

Fig. 2. Extended PEEC model

The complex inductance matrix for the conductor system with n conductors is given by:

$$L(h_{eff}) = L_{freespace} - L_{image} \quad (22)$$

$L_{freespace}$ is the inductance matrix of physical conductors in free space. L_{image} is the mutual inductance matrix between physical and image conductors. The calculation of L_{image} depends on the effective complex distance h_{eff}, thus $L(h_{eff})$ will be frequency and process parameters dependent.

To obtain line parameters, the complex inductance matrix can be interpreted as follows:

$$L(\omega) = Real[L(h_{eff})] \quad (23)$$

and

$$R(\omega) = -\omega Imag[L(h_{eff})] + R_{DC} \quad (24)$$

where $L(\omega)$ and $R(\omega)$ are the frequency dependent partial inductance and resistance matrix respectively. R_{DC} is a diagonal matrix including DC resistances of the physical filaments. It can be seen that $R(\omega)$ contains off diagonal terms which represent mutual resistances.

V. SPICE Compatible Reluctance-Based Model

In the previous section, we present how to obtain partial inductance matrix $L(\omega)$ and resistance matrix $R(\omega)$ by using complex image theory. However, $L(\omega)$ and $R(\omega)$ are extremely dense due to the globe effect of partial inductance coupling. Therefore, a more practical modeling approach is necessary to obtain circuit model of manageable size.

Reluctance based methods have been extensively used recently because reluctance has better locality than inductance. The partial reluctance matrix K is defined as the inverse of the partial inductance matrix L. In stead of directly calculating partial inductance matrix and inverting it to obtain partial reluctance matrix, most existing reluctance extraction tools are based on window selection algorithms, such as [15]. Those window algorithms can be easily extended to included image conductors: apply one of these algorithms to select physical conductors in a small window; if a physical segment is selected, its image will also be included.

Our frequency dependent reluctance-based interconnect model, EPEEC, is based on the combination of the extended PEEC and the above window selection algorithm. For each conductor, we calculate the small $L(\omega)$ and $R(\omega)$ for conductors within a small window after proper discretization according to conductor skin depth. Then the small $L(\omega)$ for this conductor group is inverted to obtain the small $K(\omega)$ matrix. The final circuit model is assembled by using those small $K(\omega)$ and $R(\omega)$ matrices.

Since EPEEC includes mutual resistances and reluctances, in order to avoid significant modifications on general simulation tools, we need to consider their SPICE compatible models, which can be obtained from their branch equations respectively. The branch equation of self and mutual resistances is

given by

$$V_i = \sum_{j=1}^{n} R_{ij} I_j = R_{ii} I_i + \sum_{j=1, j \neq i}^{n} R_{ij} I_j \tag{25}$$

where R_{ii} is self resistance and R_{ij} is the mutual resistance between R_{ii} and R_{jj}. Eq. (25) can be rewritten as

$$V_i = R_{ii} I_i + \sum_{j=1, j \neq i}^{n} \frac{R_{ij}}{R_{jj}} (R_{jj} I_j) \tag{26}$$

If we view $R_{ii} I_i$ as the voltage drop across the self resistance R_{ii}, V_i is then equal to the sum of the voltage drop on a self resistance R_{ii} and serially connected voltage control voltage sources (VCVS). These VCVSs are controlled by voltages on other self resistances which originally have mutual resistances with R_{ii}. Therefore, Eq. (26) can be used to construct SPICE compatible model for mutual resistances, which is shown in Figure 3.(a), where $V_{VCVS}^{R} = \sum_{j=1, j \neq i}^{n} \frac{R_{ij}}{R_{jj}} V_{jj}$.

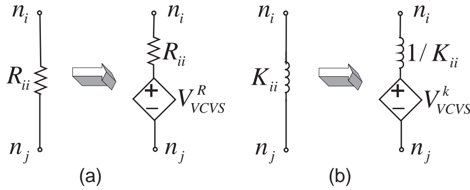

Fig. 3. SPICE Compatible Model for (a) mutual resistance (b) reluctance

SPICE compatible model for reluctance can be derived by similar method. It includes a self inductance $1/K_{ii}$ and serial VCVSs, where $V_{VCVS}^{K} = -\sum_{j=1, j \neq i}^{n} \frac{K_{ij}}{K_{jj}} V_{jj}$.

VI. Experimental Results

Extensive experimental results are reported to show the efficiency and accuracy of our new interconnect model EPEEC.

To validate the new modeling approaches and to illustrate the accuracy, we first compare the inductance values computed by the enhanced PEEC model with FastHenry [14] and a more rigorous full wave EM analysis tool, HP-Momentum. Under 20GHz, the enhanced PEEC gives inductance values that are extremely close to full wave simulation results (within 1% error) and shows over 100X speedup compared to FastHenry.

TABLE 1
INDUCTANCE VALUE COMPARISION

Frequency (GHz)	HP Momentum	FastHenry			EPEEC		
		Value (pH)	Error (%)	Time (s)	Value (pH)	Error (%)	Time (s)
5	81.1102	87.5368	7.923	558.1	81.1167	0.008	<1
10	76.8060	85.8109	11.72	569.2	76.4245	0.496	<1
15	74.0398	84.7232	14.42	588.3	73.5964	0.599	<1

The following experiment is run to show the computational complexity of EPEEC. The testing conductor system includes 604 conductor segments which are in a power/ground network from metal layer 7 to 6. Without considering the substrate, PEEC takes about 34.316s to assemble the model, while the enhanced PEEC spends about 83.131s to model the lossy substrate effect. However, they both contain 92,639 elements. While applying EPEEC by searching neighboring of shielding level one, it takes only 1.368s to obtain the circuit model with 2,794 elements.

The waveforms of extended PEEC at different frequencies are shown in Fig. 4.(a) compared to PEEC. Also the responses in Fig. 4.(b) demonstrate that EPEEC has much smaller model size while maintaining less than 3% error compared to the inductance-based enhanced PEEC model.

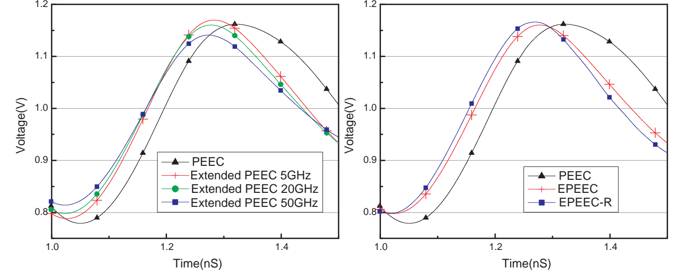

Fig. 4. The Enhanced PEEC vs. EPEEC

VII. Conclusion

A new reluctance-based interconnect model EPEEC considering the loss substrate effect is presented in this paper. It's obtained by combining an enhanced PEEC model with an extended window-based reluctance extraction algorithm. Extensive simulation results demonstrate that EPEEC has extremely high accuracy and significantly small model size.

References

[1] A. E. Ruehli, "Inductance calculatioin in a complex integrated circuit environment," *IBM Journal of Research and Development*, Sep 1972.

[2] B. Krauter and L. T. Pileggi, "Generating sparse partial inductance matrices with guaranteed stability," *ICCAD*, Nov 1995.

[3] K. L. Shepard and Z.Tian, "Return-limited inductances: A practical approach to on-chip inductance extraction," *Computer Aided Design of Integrated Ciurcuits and Systems*, Apr 2000.

[4] K. Gala, V. Zolotov, R. Panda, B. Young, J. Wang, and D. Blaauw, "On-chip inductance modeling and analysis," *DAC*, Jun 2000.

[5] A. Devgan, H. Ji, and W. Dai, "How to efficiently capture on-chip inductance effects:introducing a new circuit element k," *ICCAD*, 2000.

[6] H. Ji, A. Devgan, and W. Dai, "Ksim: A stable and efficient rkc simulator for capturing on-chip inductance effect," *ASPDAC*, Jun 2001.

[7] R. Gharpurey and R. G. Meyer, "Modeling and analysis of substrate coupling in integrated circuits," *Custom Integrated Circuits Conference*, May 1995.

[8] B. R. Stanisic, N. K. Verghese, R. A. Rutenbar, L. R. Carley, and D. J. Allstot, "Address sunstrate coupling in mixed-mode ic's simulation and power distribution synthesis." *Solid-State Circuits*, 1994.

[9] T.-H. Chen, C. Luk, H. Kim, and C. C.-P. Chen, "Supreme: Substrate and power-delivery reluctance-enhanced macromodel evaluation," *ICCAD*, 2003.

[10] P. R. Bannister, "Applications of complex image theory," *Radio Science*, Aug 1986.

[11] A. Weisshaar and H. Lan, "Accurate closed-form expressions for the frequency-dependent line papameters of on-chip interconnects on lossy silicon substrate," *IEEE MTT-S International Microwave Symposium Digest*, May 2001.

[12] A. Weisshaar, H. Lan, and A. Luoh, "Accurate closed-form expressions for the frequency-dependent line papameters of coupled on-chip interconnects on lossy silicon substrate," *IEEE Trans. Adv. Packaging*, 2002.

[13] D. Melendy and A. Weusshaar, "A new scalable model for spiral inductors on lossy silicon substrate," *Microwave Symposium Digest*, 2003.

[14] M. Kamon, M. J. Tsuk, and J. K. White, "Fasthenry: A multipole-accelerated 3-d inductance extraction program," *DAC*, Jun 1993.

[15] G. Zhong, C.-K. Koh, V. Balakrishnan, and K. Roy, "An adaptive window-based susceptance extraction and its efficient implementation," *DAC*, Jun 2003.