# RC-in RC-out Model Order Reduction Accurate Up to Second Order Moments 

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#### Abstract

In this paper, we present a RC-in RC-out model order reduction method which takes RC circuits and accurate reduced models which can be realized using passive RC elements. The reduced models are accurate up to 2 nd order moment and hence are more accurate than the first order moment matching based algorithm [3], [4], [5]. The runtime and reduction ratios of our method are not dependent on the number of ports, which can be very large for tightly coupled interconnects. Extensive SPICE simulations show the average accuracy of our algorithm is 5 X better than first order moment based algorithms. It also significantly improves the reduction ratio by $50 \%$ comparing the first order moment based algorithm for the same accuracy.


I. Pattern Matching Rule-Based Reduction Procedure
In this section, we present our rule-based realizable model order reduction method. We first develop many circuit primitives which can match predetermined second order moments and then recursively search the circuits to replace such circuit patterns which can be replaced by these primitives without losing much accuracy. L2-Reduction and C2-Reduction are the rules we newly proposed.

## 1) L2-Reduction:

The basic primitive of L2-reduction is a $2-\pi$ model as


Fig. 1. L-2 Reduction (a) Before reduction (b)After reduction.
shown in Figure 1.b. L2-reduction replaces two-port circuit such as shown in Figure 1.a with Figure 1.b. The replacement is repeated till no further reduction is possible. Note that we can also perform the reduction once for serially connected RC wire segments rather than one reduction at a time. L2-Reduction is more accurate than the single order moment matching technique (L1 reduction) since it matches two moments rather than one. It matches second order moments from both directions, total resistance, and total capacitance as the original circuit. Given total resistance ( $R^{\prime}$ ), total capacitance ( $C^{\prime}$ ), Elmore delay form left to right $\left(M_{1 R}\right)$ and from right to left $\left(M_{1 R}\right)$, second order moments from left to right $\left(M_{2 L}\right)$ and from right to left $\left(M_{2 L}\right)$ for a given two-port circuit such as shown in Figure 1.a. L2-Reduction constructs a $2-\pi$ circuit as shown in Figure 1.b where all the above parameters are matched. Let $C_{1}, C_{2}, C_{3}, R_{1}, R_{2}$ be the capacitances and resistances values in Figure 1.b. We have the following equations:

$$
\begin{align*}
R_{1}+R_{2} & =R^{\prime}  \tag{1}\\
C_{1}+C_{2}+C_{3} & =C^{\prime}  \tag{2}\\
R_{1}\left(C_{2}+C_{3}\right)+R_{2} C_{3} & =M_{1 R} \\
R_{1} C_{1}+R_{2}\left(C_{1}+C_{2}\right) & =M_{1 L}  \tag{3}\\
R_{1}\left(C_{2} R_{1}\left(C_{2}+C_{3}\right)+C_{3} M_{1 R}\right)+R_{2} C_{3} M_{1 R} & =M_{2 R}
\end{align*}
$$

(5)

$$
\begin{align*}
R_{2}\left(C_{2} R_{2}\left(C_{1}+C_{2}\right)+C_{1} M_{1 L}\right)+R_{1} C_{1} M_{1 L} & =M_{2 L}  \tag{6}\\
\left(M_{2 L}-M_{1 L}^{2}\right) & =P \\
\left(R^{\prime 2} M_{1 R} C^{\prime}-R^{\prime} M_{1 R} M_{1 L}-M_{2 R} R^{\prime}\right) & =K
\end{align*}
$$

After rearranging the terms, and substituting for $P$ and $K$ we get

$$
\begin{align*}
& C_{1}^{4}\left(K R^{\prime 2}\right)+C_{1}^{3}\left(-2 M_{1 L} R^{\prime} K+P R^{\prime 2} M_{1} R\right) \\
&+ C_{1}^{2}\left(P^{2} R^{\prime}-P R^{\prime} M_{1 R} M_{1 L}-P C^{\prime} R^{\prime 2} M_{1 R}+\right. \\
&\left.M_{2 R} R^{\prime} P+K M_{1 L}^{2}\right)+C_{1}\left(-P^{2} R^{\prime} C^{\prime}-P^{2} M_{1 L}\right. \\
&+\left.P M_{1 R} M_{1 L} R^{\prime} C^{\prime}-P M_{2 R} M_{1 L}\right)+P^{2} M_{1 L} C^{\prime}=0 \tag{7}
\end{align*}
$$

After obtaining $C_{1}$ from the analytical solutions of the above equation, we use the following theorem to obtain the value of $R_{1}, R_{2}, C_{2}, C_{3}$.

Theorem 1: Let $R_{1}^{*}=\frac{M_{2 L}-M_{1 L}^{2}}{C_{1}^{*}\left(R^{\prime} C_{1}-M_{1 L}\right)}, R_{2}^{*}=R^{\prime}-R_{1}^{*}$, $C_{2}^{*}=\frac{M_{1 R}-R_{1}\left(C^{\prime}-C_{1}^{*}\right)}{R_{2}}$, and $C_{3}^{*}=C^{\prime}-C_{1}^{*}-C_{2}^{*}$, respectively.

We have $C_{1}^{*}, C_{2}^{*}, C_{3}^{*}, R_{1}^{*}$, and $R_{2}^{*}$ satisfy the Equation set (1-6).
Note that a fourth order equation can be analytically solved. Hence the runtime to compute the roots for Equation set (1-6) is quite small. In our implementation, we compute all the four roots of equation (7) and use the most accurate real positive root that makes all corresponding parameters real and positive.
2) C2-Reduction:

The basic primitive of C2-reduction is a 2 -sided- $2-\pi$


Fig. 2. C-2 Recution (a) Before reduction (b)After reduction. model as shown in Figure 2.b. Our algorithm replaces
a multi-port circuit such as the one shown in Figure 2.a model as shown in Figure 2.b. Our algorithm replaces
a multi-port circuit such as the one shown in Figure 2.a with Figure 2.b.The reduced model matches all the following parameters: total resistance $\left(R^{\prime}\right)$, ground capacitance $\left(C_{g}^{\prime}\right)$, total cross-coupled capacitance $\left(C_{x}^{\prime}\right)$, and the Elmore delay and second moment from left to right and from
right to left for the full model $\left(M_{1 R}, M_{2 R}, M_{1 L}\right.$, and, $\left.M_{2 L}\right)$ more delay and second moment from left to right and from
right to left for the full model $\left(M_{1 R}, M_{2 R}, M_{1 L}\right.$, and, $\left.M_{2 L}\right)$ , and the Elmore delay and second moment from left to right and from right to left for the upper $\pi$ model $\left(X_{1 R}, X_{2 R}, X_{1 L}\right.$, and,$\left.X_{2 L}\right)$. Although there are over 10 simultaneous nonlinear equations to solve, we partitioned the equations into two sets and resolve them sequentially. The first set of equations will be used to obtain the reduced L2 circuit for the original circuit with the coupled
and grounded capacitance lumped together. The second set of equations will be used to determine the distribution of the coupled and grounded capacitance for each node for the L2 circuit obtained from the first step. We now summarize this procedure as follows: At the first step, we lump each ground capacitance with the coupled capacitance at the same node. After this process, the new problem becomes the same as L2-reduction problem. These equations can be written as follows:

$$
\begin{aligned}
R_{1}+R_{2} & =R^{\prime} \\
C_{1}+C_{2}+C_{3}+C_{x 1}+C_{x 2}+C_{x 3} & =C_{g}^{\prime}+C_{x}^{\prime} \\
R_{1}\left(C_{2}+C_{3}+C_{x 2}+C_{x 3}\right)+R_{2}\left(C_{3}+C_{x 3}\right) & =M_{1 R} \\
R_{1}\left(C_{1}+C_{x 1}\right)+R_{2}\left(C_{1}+C_{2}+C_{x 1}+C_{x 2}\right) & =M_{1 L} \\
R_{1}\left(\left(C_{2}+C_{x 2}\right) R_{1}\left(C_{2}+C_{x 2}+C_{3}+C_{x 3}\right)+\right. & \\
\left.\left(C_{3}+C_{x 3}\right) M_{1 R}\right)+R_{2}\left(C_{3}+C_{x 3}\right) M_{1 R} & =M_{2 R} \\
R_{2}\left(\left(C_{2}+C_{x 2}\right) R_{2}\left(C_{1}+C_{2}+C_{x 1}+C_{x 2}\right)+\right. & \\
\left.\left(C_{1}+C_{x 1}\right) M_{1 L}\right)+R_{1}\left(C_{1}+C_{x 1}\right) M_{1 L} & =M_{2 L}
\end{aligned}
$$

We first utilize Theorem 1 to solve the above simultaneous equations to obtain $R_{1}, R_{2}$, and the lumped total capacitance in each node $C_{1}+C_{x 1}, C_{2}+C_{x 2}$, and $C_{3}+C_{x 3}$. At the second step, we find the exact values of the cross-3coupled capacitances. The cross-coupled capacitance values $C_{x 1}$, $C_{x 2}$, and $C_{x 3}$ are obtained by solving the following simultaneous equations:

$$
\begin{aligned}
& C_{x 1}+C_{x 2}+C_{x 3}=C_{x}^{\prime} \\
& R_{1}\left(C_{x 2}+C_{x 3}\right)+R_{2} C_{x 3}=X_{1 R} \\
& R_{1} C_{x 1}+R_{2}\left(C_{x 1}+C_{x 2}\right)=X_{1 L} \\
&(10) \\
& R_{1}\left(C_{x 2} R_{1}\left(C_{x 2}+C_{x 3}\right)+C_{x 3} X_{1 R}\right)+R_{2} C_{x 3} X_{1 R}=X_{2 R} \\
& R_{2}\left(C_{x 2} R_{2}\left(C_{x 1}+C_{x 2}\right)+C_{x 1} X_{1 L}\right)+R_{1} C_{x 1} X_{1 L}=X_{2 L}
\end{aligned}
$$

Equation (8) preserves the total coupled capacitance. Equations (9)-(10) preserve the bidirectional Elmore delays caused by the coupled capacitance. and the bidirectional second order moments. The solutions of the above equations are as follows:

$$
\begin{array}{r}
C_{x 2}=-\frac{R_{1} R^{\prime}\left(X_{1 L}^{2}-X_{2 L}\right)-R_{2} R^{\prime}\left(X_{1 R}^{2}-X_{2 R}\right)}{R_{1}^{2} R_{2} X_{1 L}-R_{1} R_{2}^{2} X_{1 R}} \\
C_{x 3}=\frac{X_{1 R}-R_{1} C_{x 2}}{R^{\prime}}, C_{x 1}=\frac{X_{1 L}-R_{2} C_{x 2}}{R^{\prime}}
\end{array}
$$

## II. Experimental Results

We extensively tested the accuracy and reduction ratio for all reduction methods. Table I shows the accuracy comparison between various reduction methods on hundreds of carefully randomly generated circuits. All numerical data are based on SPICE simulation. It shows that the average accuracy of L2-Reduction is $0.36 \%$ while single moment matching technique ( L 1 reduction) is $3.0 \%$. Table II shows the accuracy and reduction ratio comparisons between L2Reduction and L1 reduction for a fixed accuracy or for a fixed reduction percentage. It shows that second-moment accurate reduction methods give over 5X improvement in accuracy for fixed reduction ratio and obtain over $50 \%$ improvement in reduction ratio for fixed accuracy requirements. Figure 3 shows the SPICE simulation results of 2000-node clock tree example before and after the circuit was reduced using L2-Reduction obtained from [1]. The difference between the two curves is negligible. Figure 4 gives the plot of the error distributions for L2-Reduction. It shows that the error is always within $1 \%$. Figure 5 plots the runtime versus the number of elements.

| Reduction | Error Comparison |
| :---: | :---: |
| L1 | $2.816 \%$ |
| L2 | $0.369 \%$ |
| C2 | $1.1085 \%$ |

TABLE I
Comparison of Accuracy of various reduction methods

| Reduction <br> Type | Comparison with |  |
| :---: | :---: | :---: |
|  | Reduction at $60 \%$ | Error at 0.04\% |
|  | Error | Reduction |
| First moment | $0.8 \%$ | $5 \%$ |
| Second moment | $0.04 \%$ | $57 \%$ |

TABLE II
COMPARISON OF SECOND ORDER(L2) AND FIRST ORDER(L1) MOMENT MATCHING


Fig. 3. The Spice simulation of the original file and the reduced file


Fig. 4. A plot of the error percentages for L2 reduction


Fig. 5. The plot of runtime versus the number of elements

## References

[1] R. S. Tsay, "An exact zero-skew clock routing algorithm" IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, February 1993.
[2] Jacob White and Alberto Sangiovanni-Vincentelli, "Relaxation Techniques for the Simulation of VLSI Circuits", Kluwer Academic Publishers, Boston/Dordrecht/London, October 1986.
[3] A. Devgan and P. R. O'Brien, "Realizable Reductoin for RC Interconnect Circuits", Proc. ICCAD, 1999.
[4] B. N. Sheehan, "TICER: Realizalbe Reduction of Extracted RC Circuits", Proc. ICCAD, 1999.
[5] A. J. Genderen and N. P. van der Meijs, "Space user's manual,Space tutorial,Space 3D capacitance extraction user's manual,"Tech. Rep., Delft University of Technology, Dept of EE, Delft, The Netherlands,1995.

